Features

Serial Interface

- Supports two independent full-duplex HDLC channels (PT7A6526: one channel, PT7A6525/6525L: two channels)
  - On-chip clock generation or external clock source
  - On-chip DPLL type clock recovery for each channel
  - Two independent baud-rate generators (PT7A6526: one baudrate generator)
  - Independent time-slot assignment for each channel with programmable time-slot length (1 to 256 bit)
- Provides up to 64 bytes each for Transmit and Receive FIFOs
- Various data encoding modes
- Modem control lines (RTS, CTS, CD)
- Supports bus configuration by Collision Resolution
- Programmable bit inversion
- Data rate up to 8Mb/s
- Transparent Mode selectable
- Power Supply: 5V (6525/6526) or 3.3V (6525L)
- Available Package: 44-pin PLCC and 44-pin MQFP (PT7A6525 only)

Applications

- Data link controller and protocol generators
- Digital sets, PBXs and private packet networks
- C-channel controller of data network interface circuits
- D-channel controller for ISDN basic access
- Interprocessor communications

Protocol Support

- Supports LAPB/LAPD/SDLC/HDLC protocol in Auto Mode
- Handles Bit-Oriented functions in all modes
- Modulo-8 or modulo-128 operation
- Programmable maximum packet size checking
- Programmable time-out and retry conditions

Microprocessor Interface

- Efficient transfer of data blocks by DMA or Interrupt Request
- 8-bit demultiplexed or multiplexed bus interface
- Suitable for Intel or Motorola microprocessor

Ordering Information

Part No.	Package
PT7A6525J	44-Pin PLCC
PT7A6525LJ	44-Pin PLCC
PT7A6526J	44-Pin PLCC
PT7A6525M	44-Pin MQFP
PT7A6525JE	Lead free 44-Pin PLCC
PT7A6525LJE	Lead free 44-Pin PLCC
PT7A6526JE	Lead free 44-Pin PLCC

Introduction

The PT7A6525/6525L/6526 are designed to implement high-speed communication links using HDLC protocols. They profoundly reduce the hardware and software overhead needed for serial synchronous communications.

The PT7A6525/6525L supports two completely independent full-duplex HDLC channels (channel A and channel B), while the PT7A6526 supports only one (channel B). For each channel, there are an internal Oscillator, Baud-Rate Generator (BRG), Digital Phase-Locked Loop (DPLL), Time-Slot Assignment (TSA) Circuitry, and a Link Controller to support various layer-1 functions. They also directly support the X.25 LAPB, the ISDN LAPD and SDLC (normal response mode) protocols and are capable of handling a large set of layer-2 protocol functions independently.

The data link controller handles all functions necessary to establish and maintain an HDLC data link, such as

- Flag insertion and detection,
- Bit stuffing,
- CRC generation and checking, and
- Address field recognition.

Associated with each serial channel are a set of independent command and status registers and 64-byte FIFOs each for the transmit and receive directions. Data blocks from / to system memory can be transferred by either Interrupt Request or Direct Memory Access (DMA).

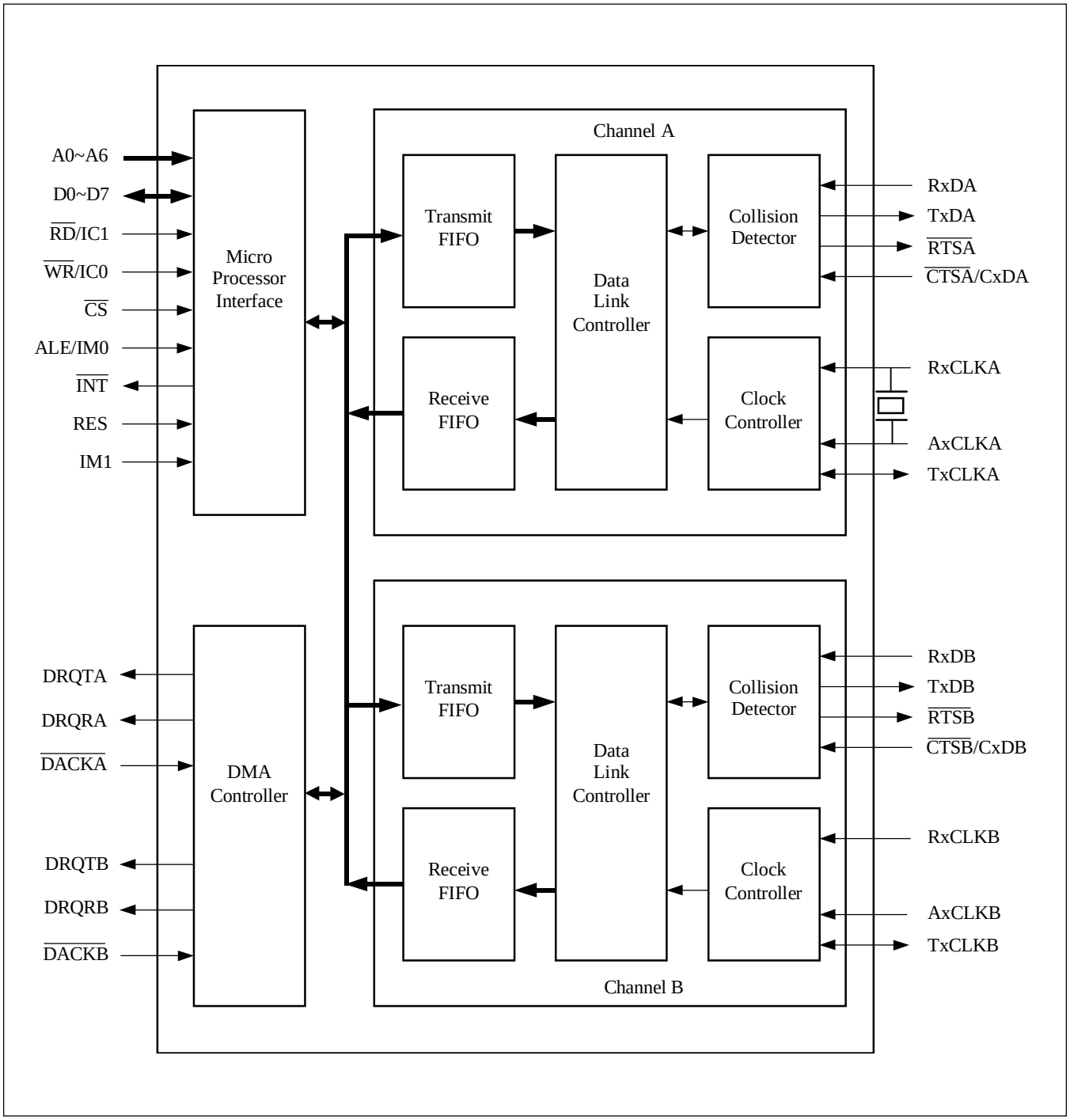
Associated with each serial channel are its own separate transmit and receive DMA request lines. Thus, the PT7A6525/6525L has a 4-channel DMA interface.

A variety of programmable telecom-specific features allow the PT7A6525/6525L/6526 to be widely used in time-slot oriented PCM systems, systems designed for packet switching, and ISDN applications.

Contents

Block Diagram

Figure 1. Block Diagram



Pin Information

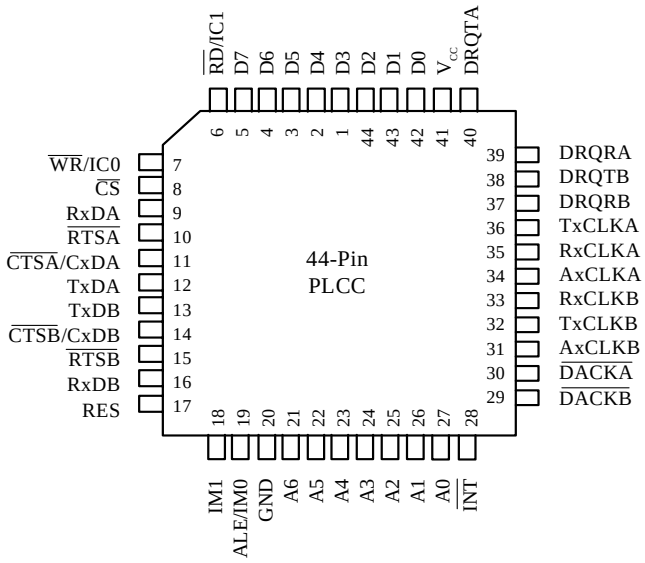
Pin Assignment

Table1. Pin Assignment

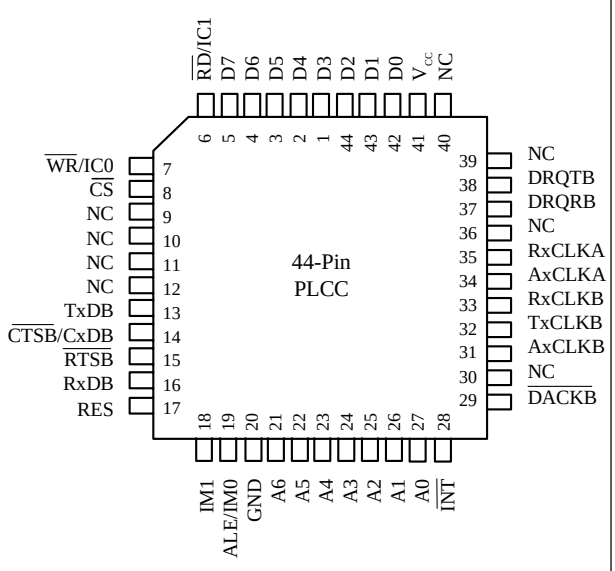
Group	Symbol	Function
Chip Clock	AxCLKA, AxCLKB, TxCLKA, TxCLKB, RxCLKA, RxCLKB	Clock
Power & Ground	GND, V_{CC}	Power
Microprocessor Interface	D0-D7, A0-A6, $\overline{RD}$/IC1, $\overline{WR}$/IC0, $\overline{CS}$, ALE/IM0, $\overline{INT}$, RES, IM1	Data or Control
I/O Interface	RxDA, TxDA, TxDB, RxDB	Serial Data
DMA Interface	DRQTA, DRQRA, $\overline{DACKA}$, $\overline{DACKB}$, DRQTB, DRQRB	DMA Control
Others	$\overline{RTSA}$, $\overline{CTSA}$/CxDA, $\overline{CTSB}$/CxDB, $\overline{RTSB}$	Depending on Bus Configurations

Pin Configuration

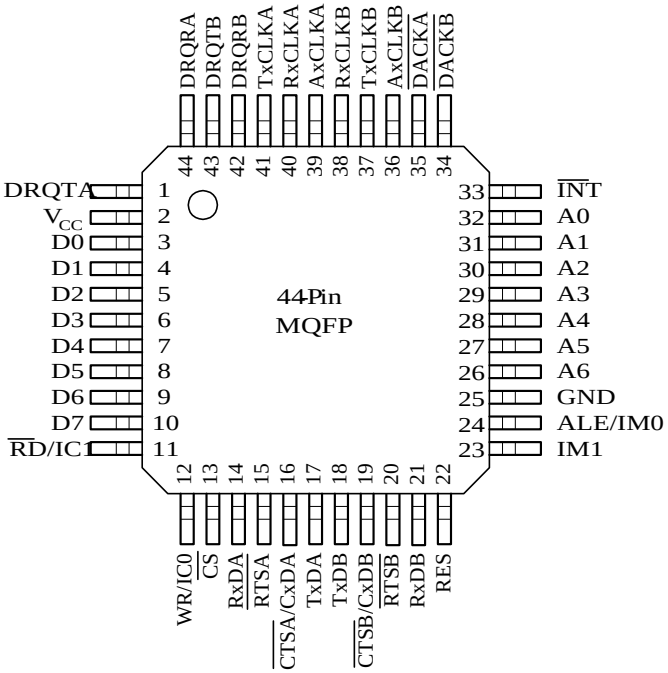
Figure 2. Pin Configuration



PT7A6525J/6525LJ



PT7A6526J



PT7A6525M

Top view

Pin Description

Table 2. Pin Description

Pin	Name	Type	Description
42~44 1~5	D0~D2 D3~D7	I/O	**8-bit data bus:** Bidirectional tristate lines interfacing with the system's data bus
6	$\overline{RD}$/IC1	I	**Read,** Intel bus mode Indicates a read operation. When the device is selected, a low input enables the bus driver to put data to the data bus from an internal register addressed via A0-A6. If the device is in DMA Mode, a low input enables the bus driver to put data to the data bus from the respective receive FIFO, while A0-A6 are ignored. **Input Control 1**, Motorola bus mode IC1 could be E or DS signal depending on the level of the IM0 pin to control read/write operation. IM0=LOW, IC1=E (Active HIGH); IM0=HIGH, IC1=DS (Active LOW)
7	$\overline{WR}$/IC0	I	**Write**, Intel Bus mode Indicates a write operation. When the chip is selected, a low input enables the data on the data bus to be written to an internal register. If the chip is in DMA Mode, a low input enables the data on the data bus to be written to the top of the corresponding transmit FIFO. **Input control 0,** Motorola bus mode To distinguish between read or write operations.
8	$\overline{CS}$	I	**Chip Select:** A low signal selects the device for a read/write operation.
9 16	RxDA RxDB	I	**Receive data:** Serial data is received on these pins at standard TTL or CMOS levels. (Note: By the set of the bit D7 in CCR2, RxDs and TxDs can be exchanged. Refer to the description of CCR2.)
10 15	$\overline{RTSA}$ $\overline{RTSB}$	O	**Request to sen**d: When the RTS bit in the mode register is set, the RTS signal goes low. When RTS is reset, the signal goes high if the transmission has finished, and there is no further request for transmission. In a bus configuration, this pin can be programmed via CCR2 to: - go low during the actual transmission of a frame shifted by one clock period, excluding collision bits, - go low during the reception of a data frame, - stay always high (RTS disabled).
11 14	$\overline{CTSA}$/ CxDA $\overline{CTSB}$/ CxDB	I	**Clear to Send** A low on the CTS input enables the corresponding transmitter. Additionally, an interrupt may be issued if a state transition occurs at the CTS pin (programmable feature). If no "Clear To Send" function is required, the CTS inputs can be connected directly to GND. **Collision Data,** (channel A/channelB), in bus configuration This pin serves as CxDA/B. The external serial bus must be connected to the corresponding CxDA/B pin for collision detection.

Table 2. Pin Description (Continued)

Pin	Name	Type	Description
12 13	TxDA TxDB	O	**Transmit data:** Transmit data is shifted out via these pins at standard TTL or CMOS levels. These pins can be programmed to work either as push-pull, or open drain outputs supporting bus configurations.(Note: By the set of bit D7 in CCR2, RxDs and TxDs can be exchanged. Refer to the description of CCR2.)
17	RES	I	**Reset:** A high signal on this input forces the chip into the reset state. The chip is in power-up mode during reset and in power-down mode after reset. The minimum pulse width is 1.8µs.
18	IM1	I	**Input mode 1:** By connecting this pin to either GND or $V_{CC,}$ the bus interface can be adapted to either Intel or Motorola environment. IM1 = LOW: Intel bus mode IM1 = HIGH: Motorola bus mode
19	ALE/ IM0	I	**Address latch enable,** Intel bus mode A high on this line indicates an address on the external address/data bus which will select one of the chip's internal registers. The address is latched by the chip with the falling edge of ALE. This allows the chip to be directly connected to a microprocessor with multiplexed address/data bus. The address input pins A0-A6 must be externally connected to the data bus pins (D0-D6 for 8-bit microprocessors, D1-D7 for 16-bit microprocessors, i.e., multiply all internal register addresses by 2). This pin should be connected to high for a de-multiplexed bus. **Input mode 0,** Motorola bus mode In Motorola Bus Mode, the level at this pin determines the function of the IC1 pin (see description of pin 6).
20	GND	Ground	**Ground**
27 26 25 24 23 22 21	A0 A1 A2 A3 A4 A5 A6	I	**Address bus:** These inputs interface with seven bits of the system's address bus to select one of the internal registers for read or write. They are usually connected at A0-A6 in 8-bit systems or at A1-A7 in 16-bit systems.
28	$\overline{INT}$	O	**Interrupt request**: The signal is activated when the chip requests an interrupt. The microprocessor may determine the particular source and cause of the interrupt by reading the chip's interrupt status registers. (ISTA, EXIR). $\overline{INT}$ is an open drain output; thus the interrupt request outputs of several chips can be connected to one interrupt input in a "wired-or" combination. This pin must be connected to a pull-up resistor.
30 29	$\overline{DACKA}$ $\overline{DACKB}$	I	**DMA acknowledge:** When low, this input signal from the DMA controller notifies the chip that the requested DMA cycle controlled via DRQxx (pins 37-40) is in progress, i.e., the DMA controller has achieved bus mastership from the microprocessor and will start data transfer cycles (either read or write). Together with $\overline{RD}$ if DMA has been requested by the receiver, or together with $\overline{WR}$ if DMA has been requested by the transmitter, this input works like $\overline{CS}$ to enable a data byte to be read from or written to the top of the receive or transmit FIFO of the specified channel. If $\overline{DACKn}$ is active, the input on pins A0-A6 is ignored and the FIFOs are selected. If the $\overline{DACKn}$ signals are not used, these pins must be connected to V_{CC}.

Pin Description (Continued)

Pin	Name	Type	Description
34 31	AxCLKA AxCLKB	I	**Alternative clock:** These pins realize several input functions. According to the selected clock mode, they may supply either a - CD (Carrier Detect) modem control or general purpose input, or these pins can be programmed to function as receiver enable if the ""auto start"" feature is selected (CAS bit in XBCH set). The state at these pins can be read from VSTR register. - a receive strobe signal (clock mode 1), or - a frame synchronization signal in time-slot oriented operation mode (clock mode 5), or - together with RxCLK, a crystal connection for the internal oscillator (clock modes 4,6,7, AxCLKA only).
36 32	TxCLKA TxCLKB	I/O	**Transmit clock:** The functions of these pins depend on the programmed clock mode, provided that the TSS bit in the CCR2 register is reset. Programmed as inputs (if the TIO bit in CCR2 is reset), they may supply either - The transmit clock for the respective channel (clock mode 0,2,6), or - a transmit strobe signal (clock mode 1). Programmed as outputs (if the TIO bit in CCR2 is set), the TxCLK pins supply either the - transmit clock of the respective channel which is generated by either the · baudrate generator (clock mode 2,6; TSS bit in CCR2 set), or · crystal oscilator(clock mode 3,7) or · crystal oscillator (clock mode 4), - or a tristate control signal indicating the programmed transmit time-slot (clock mode 5).
35 33	RxCLKA RxCLKB	I	**Receive clock:** The functions of these pins also depend on the programmed clock mode. In each channel, RxCLK may supply either - the receive clock (clock mode 0), or - the receive and transmit clock (clock mode 1,5), or - the clock for the baudrate generator (clock mode 2, 3), or - a crystal connection for the internal oscillator (clock mode 4,6,7,RxCLK A/B together with AxCLK A)
39 37	DRQRA DRQRB	O	**DMA request receiver:** The receiver of the device requests a DMA data transfer by activating this line. The DRQRx remains high as long as the receive FIFO requires data transfers, thus it is always blocks of data (32,16,8 or 4 bytes) that are transferred. DRQRx is deactivated immediately following the falling edge of the last read cycle.
40 38	DRQTA DRQTB	O	**DMA request transmitte**r: The transmitter of the chip requests a DMA data transfer by activating this line. The DRQTx remains high as long as the transmit FIFO requires data transfers. The number of data bytes to be transferred from system memory to the device must be written first to the XBCH, XBCL registers. It is always the blocks of data (n x 32 bytes + REST, n = 0,1,...) that are transferred until the byte count is reached. DRQTx is deactivated immediately following the falling edge of the last write cycle.
41	V_{CC}	Power	**Power supply + 5V(PT7A6525/6526) or +3.3V (PT7A6525L)**

Functional Description

General

Note: Unless otherwise stated, this entire description (including use of the word "device") refers to the PT7A6526 communication controller, which supports a single HDLC channel. It should be understood that the PT7A6525/6525L contains two such "devices".

In addition to those bit-oriented functions that are usually included to support the HDLC protocol - such as bit stuffing, CRC checking, flag and address recognition - the PT7A6526 provides substantial procedural support.

The device supports a special operating mode (Auto Mode) that processes information transfer and handshaking (HDLC protocol "I" and "S" frames) autonomously. The only restriction is that window size (number of outstanding unacknowledged frames) is limited to 1 (sufficient for most applications). The detailed communication procedures are carried out mainly between the communication controllers rather than between the processors. Therefore (in this mode), the microprocessor is kept informed about the the communication procedure status only, leaving it essentially free to manage the receive and transmit data "payload" itself. Thus, both dynamic load on the microprocessors and software expense are greatly reduced.

However, in order to maintain cost efficiency and flexibility, such functions as link setup/disconnection and recovery of protocol errors ("U" frames of HDLC protocols) are implemented by the user's software rather than by this integrated hardware.

Special operating modes are also supported; this device can transmit or receive data packets in one of up to 64 time-slots of programmable width (Clock Mode 5). Furthermore, it can transmit or receive variable data portions within a defined window of one or more clock cycles, selectable by an external strobe signal (Clock Mode 1). Such features make it especially suitable for all applications using Time Division Multiplex methods, such as time-slot oriented PCM systems, systems designed for packet switching, and ISDN applications.

An additional special feature of this device is the set of FIFO buffers used for temporary storage of data packets transferred between the serial communication interface and the parallel system bus. Also, owing to this device's overlapping input/output operation (dual-port behavior), the maximum dynamic load on the microprocessor is drastically reduced by transferring the data packets block by block via Direct Memory Access (DMA). Rather than being involved with the details of data transfer, the microprocessor need only initiate data transmission and monitor the status of completely received frames.

In addition to Point-to-Point configurations, this device directly enables Point-to-Multipoint or Multimaster configurations without additional hardware or software expense.

In Point-to-Multipoint confiurations, the PT7A6526 can be used to enable Master as well as Slave station operation. Even when operating as a slave station, the device can initiate the transmission of data at any time. An internal function block provides for Idle and Collision Detection, and Collision Resolution, which are necessary if more than one station starts transmitting simultaneously.

These features are integrated to support Multimaster configurations.

Figure 3. Frame Processing in Auto Mode

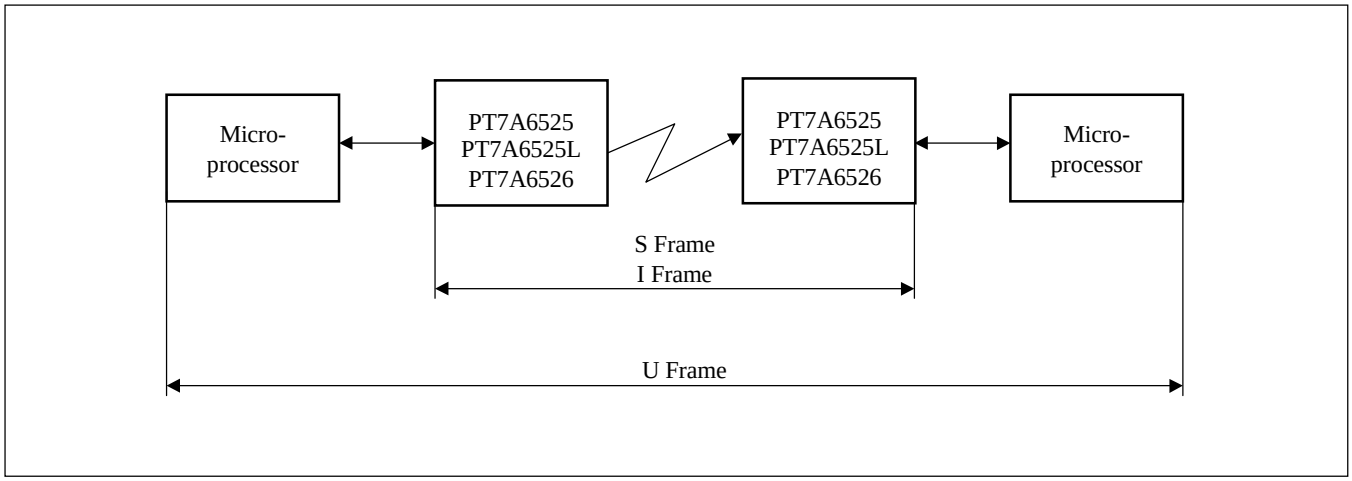
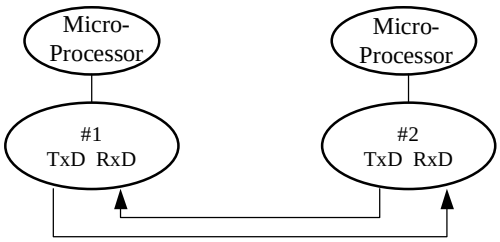
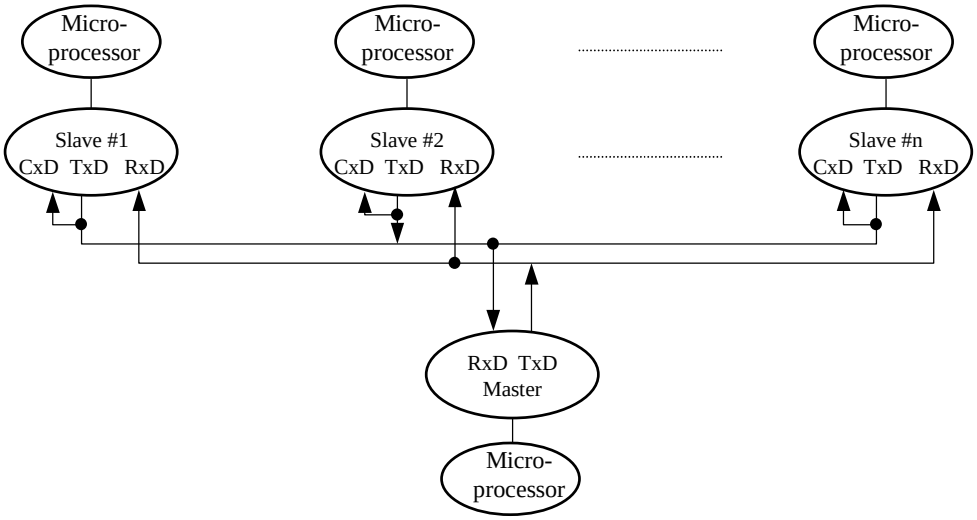


Figure 4. Link Configuration

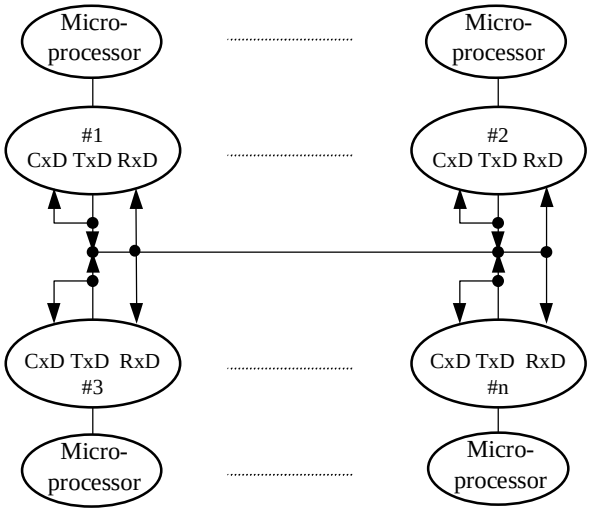
Point-to-Point Configuration



Point-to-Multipoint Configuration



Multimaster Configuration



Note: RxD-Receive Data, TxD-Transmit, CxD-Collision

Modes of Operation

There are 6 different modes of operation that can be set via the MODE register. The treatment of received frames and those that are waiting for transmission is determined by the selected modes of operation.

Auto Mode (MODE: MDS1, MDS0 = 00)

Characteristics: Window size 1, arbitrary message length, address recognition.

The PT7A6526 processes automatically all numbered frames (S, I frames) of an HDLC procedure.

The HDLC control field, data in the I field of the frames, and additional information can be read from special registers (RHCR, RSTA).

According to the selected Address Mode, the device can perform 2-byte or 1-byte address recognition. If a 2-byte address field is selected, the high address byte is compared with the fixed value FEH or FCH (group address) as well as with two individually programmable values in the RAH1 and RAH2 registers. In accordance with the ISDN LAPD protocol, bit 1 of the high address byte is interpreted as COMMAND/ RESPONSE bit (C/R) depending upon the setting of the CRI bit in RAH1 and will be excluded from the address comparison.

Similarly, two reference values can be programmed in special registers (RAL1, RAL2) for the low address byte. A valid address will be recognized if the high and low byte of the address field correspond to one of the reference values. Thus, the device can be addressed (called) with six different address combinations. However, only those frames whose addresses match with the address combination RAH1, RAL1 are processed in Auto Mode; all others are processed in Non-auto Mode. The PT7A6526 ignores such HDLC frames whose address fields do not match with any of the address combinations.

For the 1-byte address case, the RAL1 and RAL2 registers are used as reference. In accordance with the X.25 LAPB protocol, the value in RAL1 is interpreted as COMMAND and the value in RAL2 as RESPONSE.

After receiving a frame it takes 5 clock cycles to generate the response frame and to initiate transmission.

When operating in Auto Mode, the device provides substantial procedural support.

The following functions are performed:

- updating transmit and receive counter ,
- evaluation of transmit and receive counter,
- processing S commands,
- flow control with RR/RNR,
- generation of responses,
- recognition of protocol errors,
- transmitting S commands (if acknowledgement is missing),
- continuous status query of opposite station's termination after RNR has been received,
- programmable timer/repeater functions.

In addition, all unnumbered frames are forwarded directly to the microprocessor.

Non-Auto Mode (MODE: MDS1, MDS0 = 01)

Characteristics: address recognition, arbitrary window size.

All frames with valid addresses (address recognition identical to Auto Mode) are forwarded directly to the system memory.

The HDLC control field, data in the I field, and an additional status byte are temporarily stored in the RFIFO. The HDLC control field and additional information can also be read from special registers (RHCR, RSTA).

In Non-Auto Mode, all frames are processed similarly as in Auto Mode.

Transparent Mode 1 (MODE: MDS1, MDS0, ADM = 101)

Characteristics: high address byte recognition

Only the high byte of a 2-byte address field will be compared with the reference values. The entire frame, except for the first address byte, will be stored in RFIFO. RAL1 contains the second byte, and RHCR the third byte following the opening flag.

Transparent Mode 0 (MODE: MDS1, MDS0, ADM = 100)

Characteristics: no address recognition

There is no address recognition process performed, and each frame will be stored in the RFIFO. RAL1 contains the first byte, and RHCR the second byte following the opening flag.

Extended Transparent Mode 0 and Mode 1 (MODE: MDS1, MDS0 = 11)

Characteristics: fully transparent

In Extended Transparent Modes, the fully transparent data transmission/reception process without HDLC framing is performed, i.e., without FLAG generation/recognition, CRC generation/check, and bit-stuffing/removal. This allows user specific protocol variations or the usage of Character Oriented Protocols (such as IBM BISYNC).

In these modes, the transmitted data always passes through the XFIFO. In Extended Transparent Mode 0 (ADM = 0), data reception is done via the RAL1 register, which always contains the actual data byte assembled at the RxD pin. In Extended Transparent Mode 1 (ADM = 1), the received data is also shifted into the RFIFO.

In order to enable fully transparent data transfer, the RAC bit in MODE must be reset, and FFH has to be written to XAD1, XAD2, and RAH2.

Data transmission is always performed out of the transmit FIFO by directly shifting the contents of the XFIFO via the serial transmit data pin (TxD). Transmission is initiated by setting CMDR: XTF (08H); end of transmission is indicated by EXIR: EXE (40H). In the receive direction, the data currently assembled via the receive data line (RxD) is available in the RAL1 register. Additionally, in Extended Transparent Mode 1 (MODE: MDS1, MDS0, ADM = 111), the received data is shifted into the RFIFO.

If the Extended Transparent Modes are selected, the device supports the continuous transmission of the XFIFO's contents. After having written 1 to 32 bytes to the XFIFO, the commands XREP, XTF and XME (by writing 2AH to the CMDR register) force the chip to repeatedly transmit the data stored in the XFIFO via TxD pin, until a reset command (CMDR: XRES) is issued, after which continuous □1□-s are transmitted.

Note: In DMA Mode the commands XREP and XTF must be written to CMDR.

The management of received HDLC frames in various modes of operation is shown in the following table:

Table 3. HDLC Frames in Various Operation Modes

Mode	MDS1	MDS0	ADM	Received Package				
				Address2	Address1	Control	I field	CRC
Auto/16	0	0	1	Δ RAH1,2	Δ RAL1,2	# RFIFO* RHCR*	RFIFO*	RFIFO* RSTA*
Auto/8	0	0	0	Δ RAL1,2	-	# RFIFO* RHCR*	RFIFO*	RFIFO* RSTA*
Non-Auto/16	0	1	1	Δ RAH1,2	Δ RAL1,2	RFIFO* RHCR*	RFIFO*	RFIFO* RSTA*
Non-Auto/8	0	1	0	Δ RAL1,2	-	RFIFO* RHCR*	RFIFO*	RFIFO* RSTA*
Transparent 1	1	0	1	Δ RAH1,2	RFIFO* RAL1*	RFIFO* RHCR*	RFIFO*	RFIFO* RSTA*
Transparent 0	1	0	0	RFIFO* RAL1*	RFIFO* RHCR*	RFIFO*	RFIFO*	RFIFO* RSTA*

Note: RFIFO: Receive FIFO
RHCR: Receive HDLC Control Register
RSTA: Receive Status Register
RAL1,2: Receive Address Low1,2
RAH1,2: Receive Address High1,2
D: Compared with Register
#: Processed Autonomously
*: Stored to FIFO or Register
- : the byte does not exist

The management of HDLC frames to be transmitted is shown as follows.
Two different types of frames can be transmitted:

- I frames and
- Transparent frames

For I frames (command XIF via CMDR register), the address and control fields are generated autonomously by the device, and the data in the XFIFO enters into the information field of the frame. This is possible only when the device is in Auto Mode.

For transparent frames as well (command XTF via CMDR register), the address and the control fields must be sent to the XFIFO. This is possible in all operating modes and is also used in Auto Mode for sending U frames.

Table 4. Transmit Data Flow

Types	Different Parts of Frames				
	ADDR		CTRL	I	CRC
Transparent Frame	XFIFO	XFIFO	XFIFO	XFIFO	CRC Generator
I Frame	XAD1	XAD2	Auto Generate	XFIFO	CRC Generator

Procedural Support (Layer-2 Functions)

Full-Duplex LAPB/LAPD Operation

There are two modes of LAPB/LAPD operation, Full-Duplex and Half-Duplex operations:

In Full-Duplex LAPB/LAPD operation, the combined (master+slave) station transmits both commands and responses and may transmit data at any time.

• Reception of Frames

The logic processing of received S frames is performed by the PT7A6526 without interrupting the microprocessor. The microprocessor is merely informed via interrupts concerning status changes in the opposite station (receive ready/receive not ready) and protocol errors (unacceptable N(R) or S frame with I field).

I frames are also processed autonomously and checked for protocol errors. An I frame will not be accepted if an N(S) error occurs (no interrupt is forwarded to the microprocessor) but it will be immediately confirmed by an S response. If the microprocessor sets the device into a 'Receive Not Ready' status, an I frame will not be accepted (no interrupt) and an RNR response is transmitted. U frames are always stored in the RFIFO and forwarded directly to the microprocessor.

Note: The state variables N(S), N(R) are evaluated within the window size, i.e., the device checks only the LSB of the receive and transmit counter regardless of the selected modulo count.

• Transmission of Frames

The device autonomously transmits S commands and S responses in Auto Mode. Either Transparent or I frames can be transmitted by the user. The software timer must be in Internal Timer Mode in order to transmit I frames. After the frame has been transmitted, the timer is self-started,the XFIFO is inhibited, and the device waits for the arrival of a positive acknowledgement. This acknowledgement can be contained in an S or I frame.

If no positive acknowledgement is received during time *t1*, the device transmits an S command (p=1), which must be followed by an S response (f=1). If the S response is not received, the S command process will be performed n1 times before it is terminated.

Upon the arrival of an acknowledgement, or after the completion of this polling procedure, the XFIFO is enabled, and an interrupt is forwarded to the microprocessor. Interrupts may be triggered by the any of following events:
- message has been acknowledged as positive (XPR interrupt);
- message must be repeated (XMR interrupt);
- response has not been received (TIN interrupt).

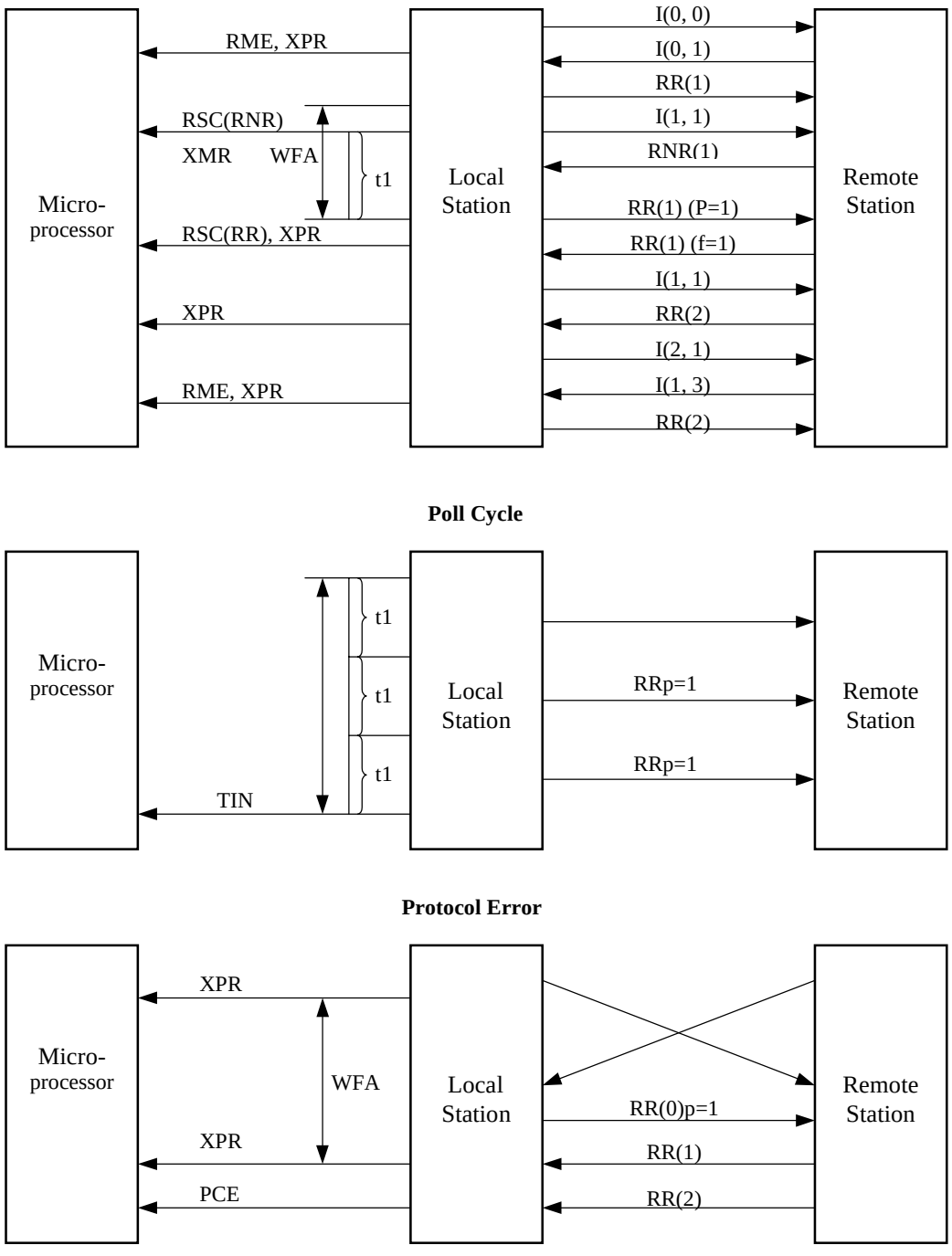
Upon arrival of an RNR frame, the software timer is started and the status of the opposite station is polled periodically after expiration of *t1*, until the status "Receive Ready" has been detected. The microprocessor is informed accordingly via interrupt. If no response is received after n1 times an interrupt will be generated (TIN interrupt).

Note: The Internal Timer Mode should be used only in the Auto Mode.

□ransparent frames can be transmitted in all operating modes. After transmission of a transparent frame the XFIFO is immediately enabled, which is confirmed by interrupt (XPR). In this case, time monitoring can be performed with the timer in the external timer mode.

The protocol process of transmit/receive frames among the microprocessor, the local station and the remote station in Auto Mode are shown in Figure 5.

Figure 5. The Protocol Process of Transmit/Receive Frames



Note: I(X, Y) = I(N(S), N(R)), RR(X) = RR(N(R)), RNR(X) = RNR(N(R))

Half-Duplex SDLC-NRM Operation

In Half-Duplex Normal Response Mode (NRM), the PT7A6526 will operate as a slave (secondary) station by setting the NRM bit in the XBCH register of the respective channel.

This mode allows transmission of responses only; the slave station may make a transmission only when instructed to do so by the master (primary) station.

The permission given by the primary station to transmit a frame is contained in an S or I frame with the poll bit (p) set.

In the point-to-multipoint configuration with a fixed master-slave relationship, the NRM mode can be used effectively to avoid collisions within the common transmission medium. It is the responsibility of the master station to poll the slave stations periodically and to manage error recovery.

The required setup for NRM operation is:

- Auto Mode with 8-bit address field selected

MODE: MDS0, MDS1, ADM = 000

- External Timer Mode

MODE: TDM = 0

- Same transmit and receive addresses; as only responses can be transmitted, i.e.

XAD1 =XAD2 = RAL1 = RAL2	← (address of slave)

Note: The broadcast address may be programmed in RAL2 if broadcasting is required.

• Reception of Frames

The reception of frames functions identically to LAPB/LAPD operation.

• Transmission of Frames

The device does not transmit S or I frames unless so instructed by an S or I frame with the poll bit set, sent by the primary station.

An I frame is readied for transmission in the PT7A6526 by the microprocessor issuing an XIF command (via CMDR), and the frame transmission will be initiated when the device receives either an

- RR, or
- I frame

with the poll bit set (p = 1).

After the frame has been transmitted (with the final bit set), the XFIFO is inhibited, and the device waits for the arrival of a positive acknowledgement.

As the on-chip timer must be operated while in External Mode (a secondary station may not poll the primary for acknowledgements), time-supervisory control must be handled by the primary station.

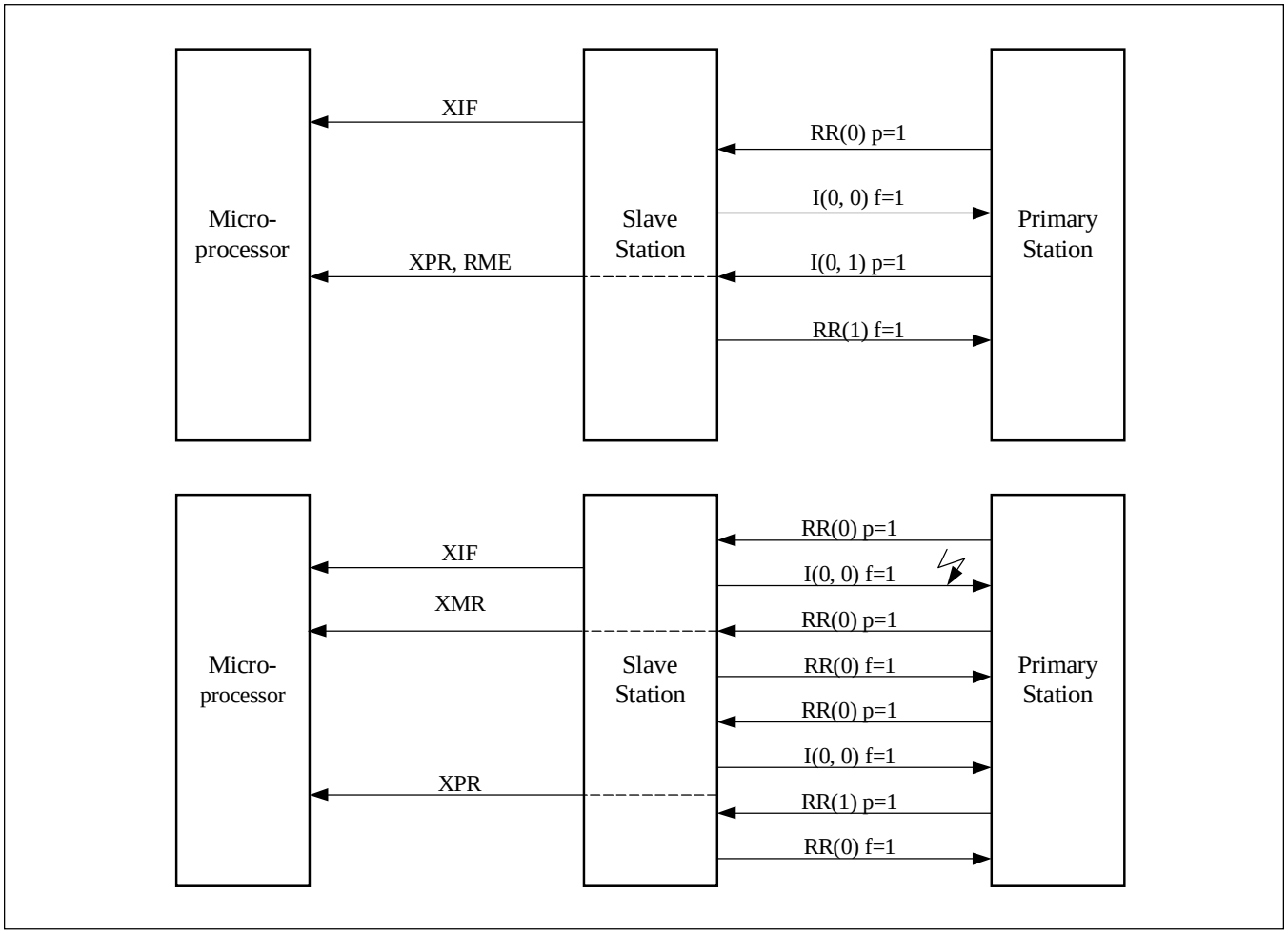
Upon the arrival of an acknowledgement, the XFIFO is enabled, and an interrupt is forwarded to the microprocessor when either
- the message has been acknowledged as positive (XPR interrupt), or
- the message must be repeated (XMR interrupt).

Additionally, the timer can be operated under microprocessor control to provide timer recovery of the slave if no acknowledgements are received at all.

Note: The transmission of transparent frames is possible only if permission to send is obtained via an S frame (p = 1) or an I frame.

Figure 6 shows the transfer of frames between primary station and slave station.

Figure 6. Transfer of Frames Between Primary Station and Slave Station



In auto mode, error frames are processed as follows.

Table 5. Error Handing

Frame Type	Error Type	Generated Response	Generated Interrupt	Rec. Status
I	CRC Error Aborted Unexpec. N(S) Unexpec. N(R)	- - S Frame -	RME RME - PCE	CRC Error Abort -
S	CRC Error Aborted Unexpec. N(R) With I Field	- - - -	- - PCE PCE	- -

Note: The station variables (V(S)), V(R)) are not changed.

Data Transfer Modes

For both transmit and receive directions, data transfer between the system memory and the PT7A6526 is controlled by either Interrupts (Interrupt Mode) or by independent microprocessor interaction using the device's 4-channel DMA interface (DMA Mode).

After RESET, the device operates in Interrupt Mode where data transfer must be done by the microprocessor. The user selects the DMA Mode by setting the DMA bit in the XBCH register. Both channels can be independently operated in either Interrupt or DMA Mode (e.g. Channel A-DMA, Channel B-Interrupt).

Interrupt Interface

Certain events within the device are indicated by means of a single interrupt output that requests the microprocessor to read status information from it. If Interrupt Mode is selected, data is transferred from/to the device.

Since only one $\overline{INT}$ request output is provided, the cause of each interrupt must be determined by the microprocessor by reading the device`s interrupt status registers (ISTA, EXIR). The structure of these registers is shown in Figure 7.

Five interrupt indications can be read directly from the ISTA register and another six interrupt indications from the extended interrupt register (EXIR).

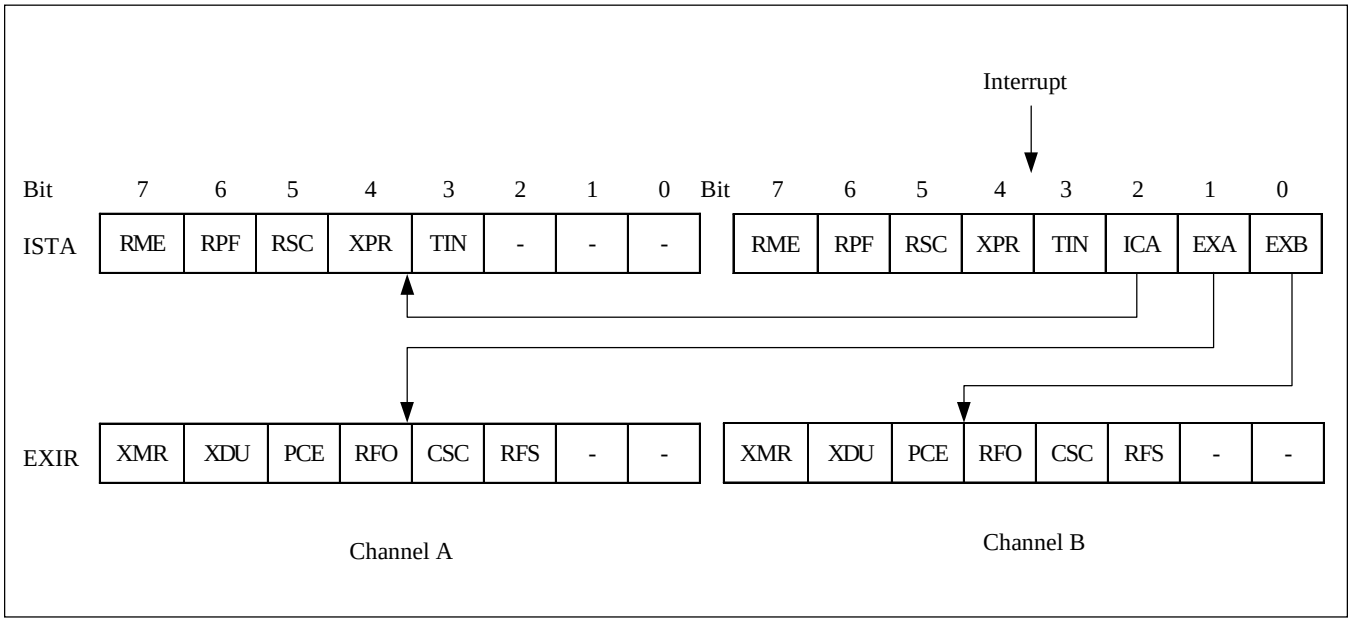
After the PT7A6525/6525L requests an interrupt by setting its $\overline{INT}$ pin to low, the microprocessor must first read the interrupt status register of channel B(ISTA-B) in the associated interrupt service routine. The three lowest order bits (bit 2-0) of ISTA-B (ICA, EXA,EXB) point are sent to those registers in which the actual interrupt source is indicated. The other bits of ISTA-B indicate that there is an interrupt source from Channel B; therefore, these bits also must always be checked. It is possible that several interrupt sources are indicated as referring to one interrupt request (e.g. if the ICA bit is set, at least one interrupt is indicated in the ISTA register of channel A). See Register Description for details.

The $\overline{INT}$ pin of the device remains active until all interrupt sources are cleared by reading the corresponding interrupt registers. Therefore it is possible that the $\overline{INT}$ pin is still active when the interrupt service routine is finished.

The interrupt sources can be logically grouped as follows:
- receive interrupts: RPF, RME, RFO, RFS;
- transmit interrupts: XPR, XMR, XDU;
- special condition interrupts: RSC, PCE, TIN, CSC.

The interrupt indication of each ISTA register can be selectively masked by setting the corresponding bit in the MASK register.

Figure 7. Interrupt Status Register



DMA Interface

The PT7A6525/6525L contains a 4-channel DMA interface for fast and effective data transfer.

For each of the two serial channels, a separate DMA Request output for the transmit (DRQT) and receive direction (DRQR), as well as a DMA Acknowledgement (DACK) input are provided.

If the DMA controller is in Level-Triggered Demand Transfer Mode, the device activates the DRQ line as long as data transfers from/to the specific FIFO are needed.

The DMA controller executes the correct number of bus cycles. Read cycles will be executed if DMA transfer has been requested by the receiver, or write cycles if DMA has been requested by the transmitter. If the DMA controller provides a DMA acknowledgement signal (input to the device`s DACK pin), for each bus cycle, the top of the applicable FIFO is implicitly selected, and neither the address (via A0-A6) nor the chip select (CS) need to be supplied (I/O to Memory transfers). If no DACK signal is supplied, normal read/write operations (providing addresses) must be performed (memory to memory transfers).

The device deactivates the DRQ line immediately after the last read/write cycle of the data transfer has started.

Continuous Transmission (DMA Mode only)

If data transfer from system memory to the device is done by DMA (DMA bit in XBCH set), the number of bytes to be transmitted is usually defined via the Transmit Byte Count registers (XBCH, XBCL: bits XBC11...XBC0).

However, after setting the □Transmit Continuously□ (XC) bit in XBCH, the byte count value will be ignored and the DMA interface of the device will continuously request for transmit data. At any time 32 bytes can be stored in the XFIFO.

This feature can be used to continuously transmit voice or data onto a PCM highway (clock mode 5/extended transparent mode). It can also be used to transmit frames exceeding the byte count that is programmable via XBCH and XBCL (frames with more than 4095 bytes).

Note: If the XC bit is reset during continuous transmission, the transmit byte count will become valid again, and the device will request the number of DMA transfers programmed via XBC11...XBC0. If this information is not provided, continuous transmission will be terminated when a data underrun condition occurs in the XFIFO ,i.e., the DMA controller will not permit more data to be transferred to the device. Moreover, the device will commence transmission of the idle pattern (continuous □1□-s) without appending the CRC check byte.

FIFO Structure

In both the transmit and receive direction, 64-byte deep FIFOs are provided for the intermediate storage of data between the serial interface and the microprocessor interface. The FIFOs are divided into two halves of 32-bytes, of which only one half is accessible to the microprocessor or DMA controller at any one time.

If a frame being received is at most 64 bytes long, all of it may be stored in the RFIFO. After the first 32 bytes have been received, the device prompts its host processor to read the 32 byte block by means of interrupt or DMA request (RPF interrupt or activation of DRQR line). This block remains in the RFIFO until confirmation acknowledging transfer of the data block is received by the device. In DMA Mode, this confirmation is implicit after 32 bytes have been read from the RFIFO. Therefore, in this mode, it is possible to read out the data block any number of times until the RMC command is issued.

Figure 8 shows the configuration of the RFIFO before and after acknowledgement.

If frames longer than 64 bytes are received, the device will repeatedly prompt to read out 32 byte data blocks via interrupt or DMA.

If there are several shorter frames, up to 17 of them may be stored in the device.

If the accessible half of the RFIFO contains a frame i (or the last part of frame i), up to 16 short frames (2 bytes for each short frame) may be stored in the other half (i+1,...,i+n) at same time, prior to frame i being fetched.

Figure 8. RFIFO Configuration (Long Frame)

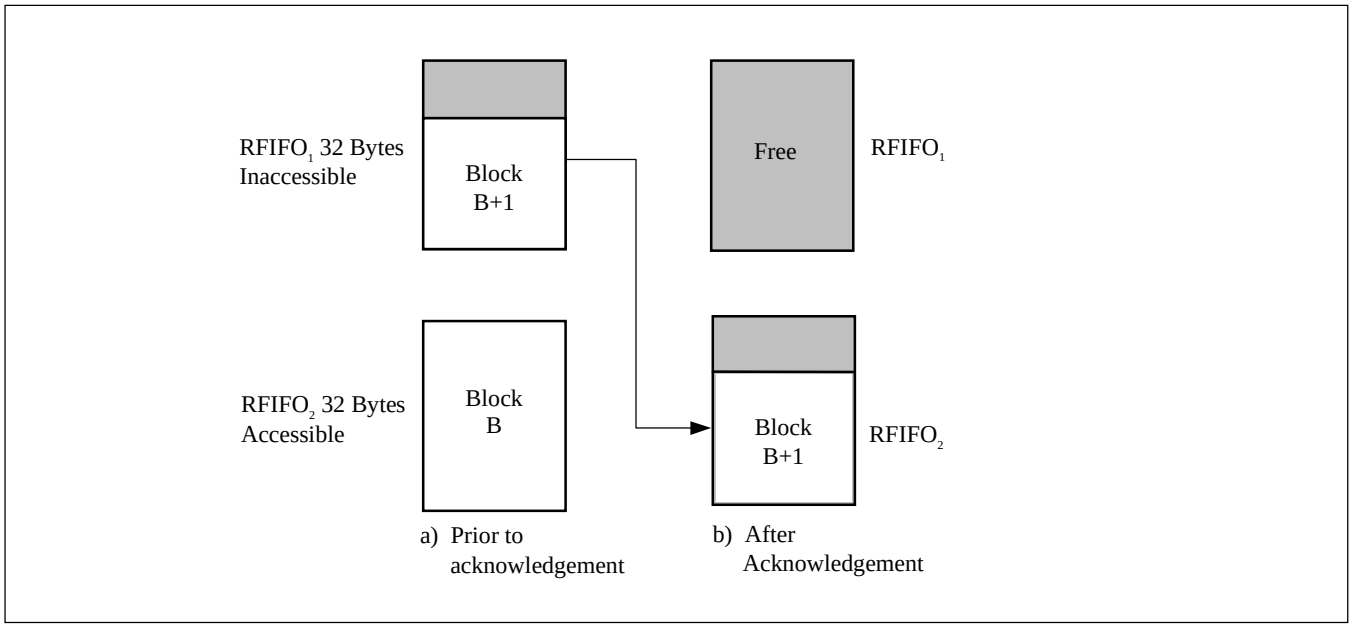
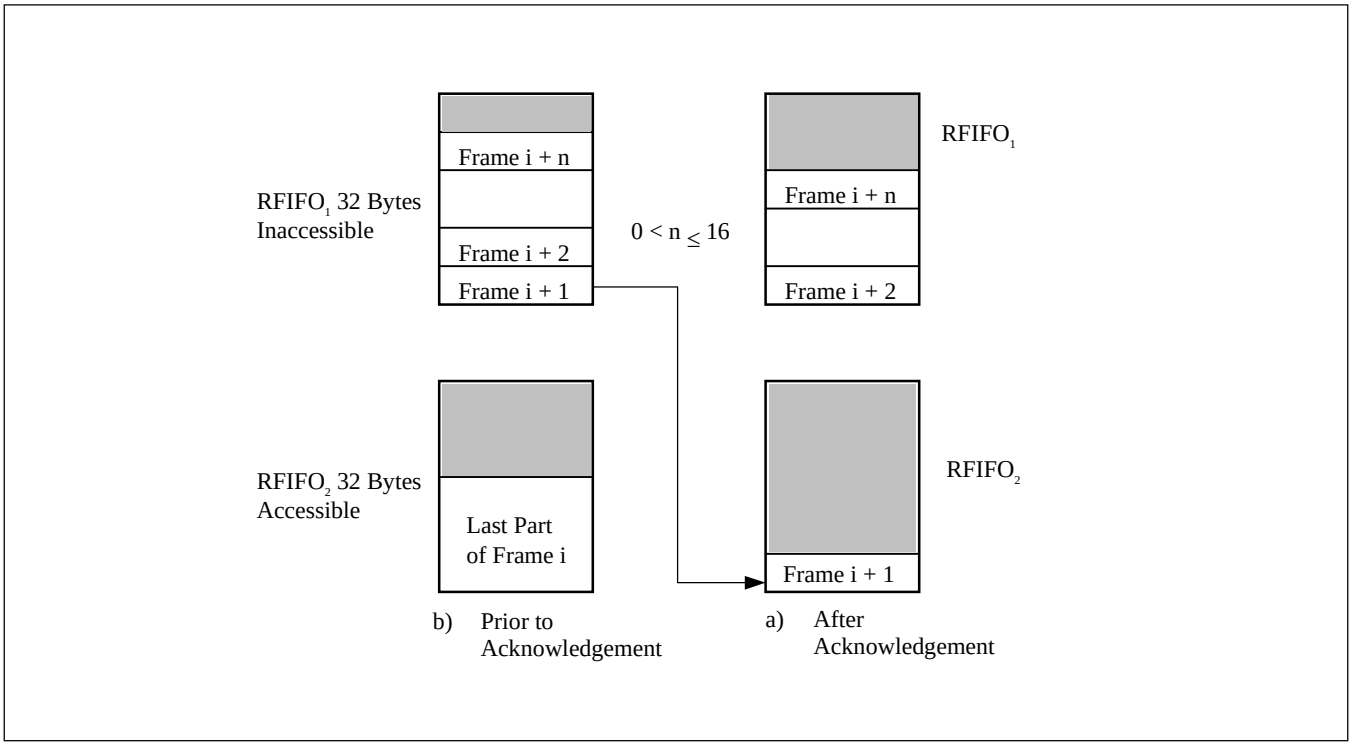


Figure 9. RFIFO Configuration (Short Frame)



Clock Modes

The PT7A6525/6525L includes an internal Oscillator (OSC), an independent Baud-Rate Generator (BRG) and Digital Phase-Locked Loop (DPLL) circuitry for each serial channel.

The transmit and receive clock can be generated either
- externally, and supplied via the RxCLK and/or TxCLK pins, or
- internally, by means of the
  - OSC and/or BRG, and
  - DPLL, recovering the Receive (and optionally Transmit) clock from the received data stream if an external crystal is connected to the RxCLKA-AxCLKA pins.

In total, there are eight different clocking modes programmable via the CCR1 register, providing a considerable variety of clock generation and clock pin functions, as shown in table 6.

Table 6. Overview of Clock Modes

Clock			
Type	**Source**	**Generation**	**Mode**
Receive Clock	RxCLK Pins	Externally	0, 1, 5
	DPLL OSC	Internally	2, 3, 6, 7 4
Transmit Clock	TxCLK Pins RxCLK Pins	Externally	0, 2, 6 1, 5
	DPLL BRG/16 OSC	Internally	3, 7 2, 6 4

The transmit clock pins (TxCLK) may also be used as an output for clock or control signals in certain clock modes if programmed as such via the CCR2 register (TIO bit set).

The clocking source for the DPLLs is always the internal BRG; the scaling factor (divider) of the BRG can be programmed through CCR2 and BGR registers within 1,2,4,6...2048.

The device system clock is always derived from the transmit clock thus eliminating the need for additional clock sources.

Clock Mode 0 (External Clocks)

Separate, externally generated receive and transmit clock are forwarded to the device via their respective pins.

Clock Mode 1 (Receive/Transmit Strobes)

Externally generated (but identical) receive and transmit clocks are forwarded via RxCLK pins. In addition, receive and transmit strobes can be connected via AxCLK and TxCLK pins respectively. The operating mode can be applied in Time Division Multiplex applications or for adjusting disparate transmit and receive data rates.

Clock Mode 2 (Receive CLock from DPLL)

The BRG is driven with an external clock (RxCLK), and it delivers a reference clock for the DPLL which then generates the receive clock. Depending on programming of the CCR2 register (TSS bit), the transmit clock will be either an external clock signal (TxCLK) or the clock delivered by the BRG divided by 16. The transmit clock can be output via TxCLK pin(CCR2: TIO = 1).

Clock Mode 3 (Receive and Transmit Clock from DPLL)

The BRG is fed with an externally generated clock via RxCLK and supplies the reference clock for DPLL which will generate both the receive and transmit clock. This clock can be output via TxCLK pin.

Clock Mode 4 (OSC-Direct)

The receive and transmit clock is directly supplied by the OSC. This clock can be output via TxCLK.

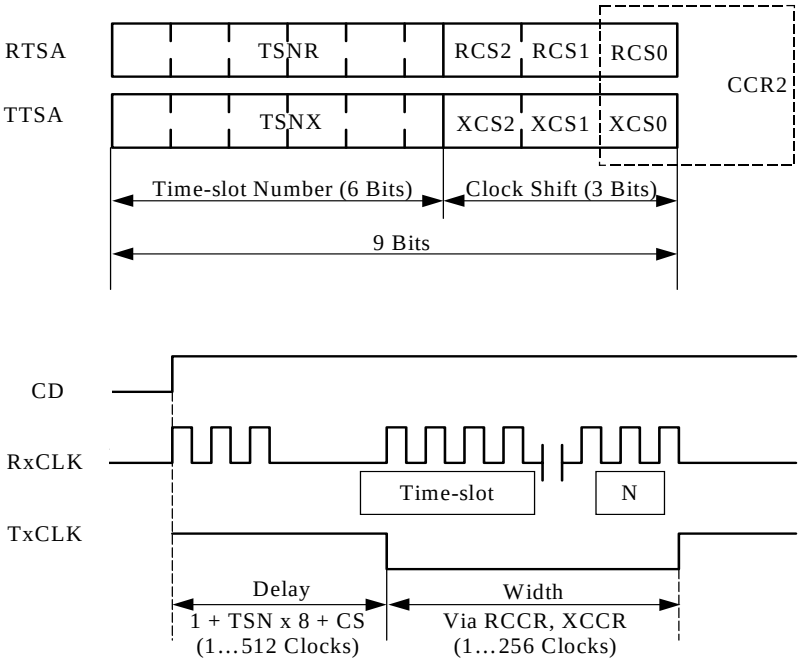
Clock Mode 5 (Time-Slots)

This operating mode is designed for application in time-slot oriented PCM systems.

The receive and transmit clocks are identical for each channel and must be supplied externally via RxCLK pins. The device receives and transmits only during certain time-slots of programmable width (1...256 bit, via RCCR and XCCR registers). The time slot locations are determined by a frame synchronization signal, which must be delivered to the device via the AxCLK pin. One of up to 64 time-slots can be programmed independently for receive and transmit direction via the RTSA, TTSA and CCR2 registers. Together with bits XCS0 and RCS0 (LSB of clock shift) in the CCR2 register, there are nine bits that determine the location of a time-slot.

According to the value programmed via these nine bits, the receive/transmit window (time-slot) starts with a delay of between 1 and 512 clock periods following the frame synchronization signal and is active during the number of clock periods programmed via RCCR, XCCR (number of bits to be received/transmitted within a time-slot) as shown below.

Figure 10. Location of Time-slots



Note:
Pin TxCLK is low during the transmit time-slot. In extended transparent mode, the time-slot width must be N x 8 bits.

$\overline{RTS}$ Signal in Clock Mode 5

In Clock Mode 5, the Request to Send ($\overline{RTS}$) control signal is deactivated after transmission of the second-to-last bit (instead of the last bit) of a closing flag, if that second-to-last bit is the last bit of a time-slot "window". In other words, $\overline{RTS}$ is inactive during transmission of the last bit of any closing flag transmitted in the next time-slot window.

$\overline{CTS}$ Signal in Clock Mode 5

In Clock Mode 5 the Clear to Send ($\overline{CTS}$) control signal is evaluated not only within the time-slot window, but also between the time-slot window $\overline{CTS}$ must be kept active even between the time-slot window until transmission of the frame has been completed. Deactivation of $\overline{CTS}$ stops data transmission immediately.

Note: When several HDLC channels are sharing the same time-slot on a bus without using Bus Collision Detection, the strobe signals (AxCLKA/B) can be used to select/deselect a particular time-slot window for an individual HDLC channel.

Figure 11. $\overline{RTS}$ Signal in Clock Mode 5

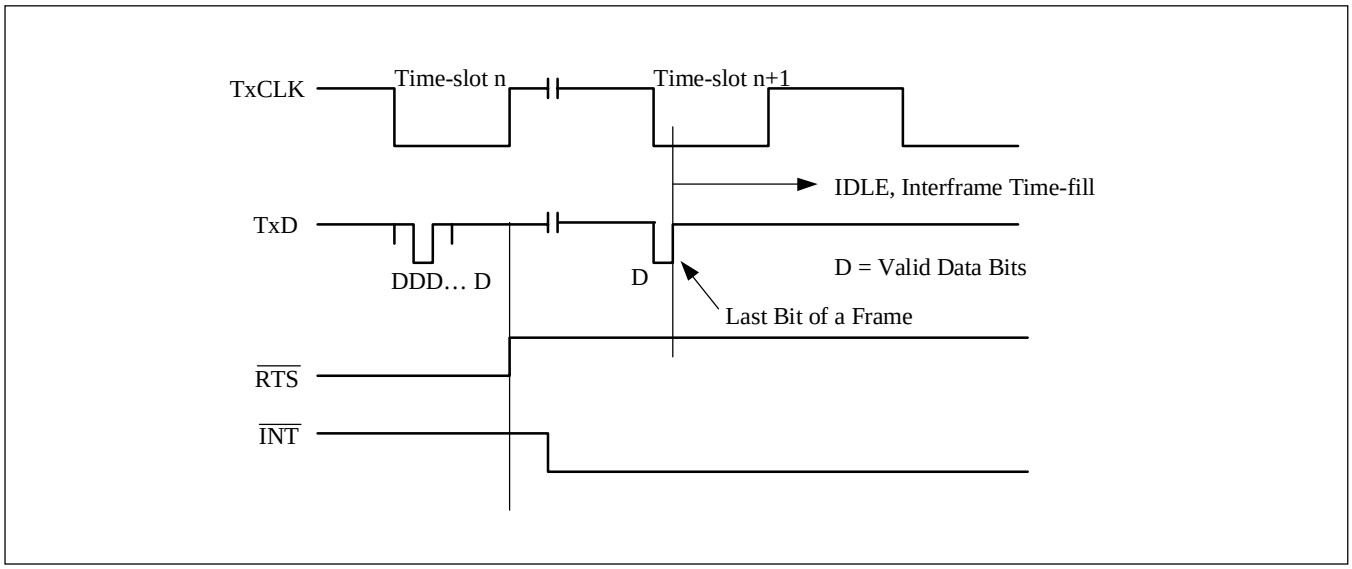
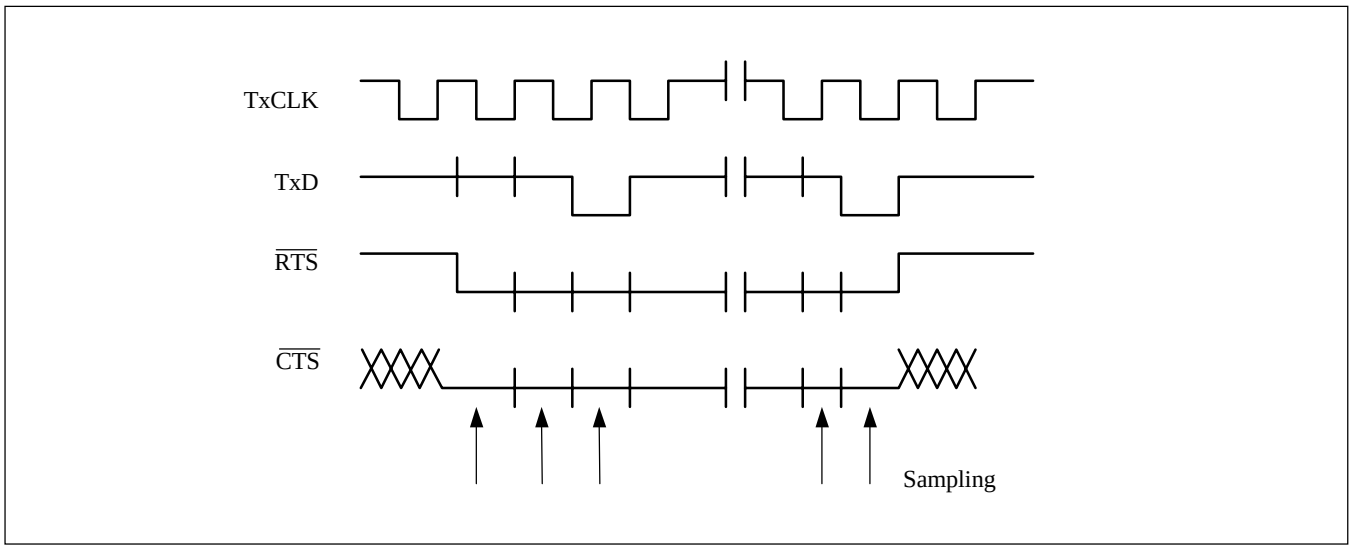


Figure 12. $\overline{CTS}$ Signal in Clock Mode 5



Clock Mode 6 (OSC - Receive Clock from DPLL)

This clock mode is identical to Clock Mode 2, except that the clock for the BRG is delivered by the OSC and must not be provided externally.

Clock Mode 7 (OSC - Receive and Transit Clock from DPLL)

Similar to Clock Mode 3, but BRG clock is provided by OSC.

Summary

The various clock mode features are summarized in Table 7.

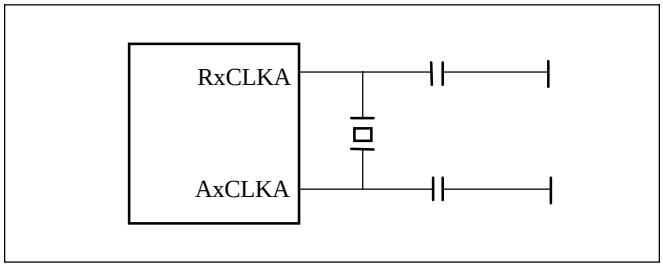
Table 7. Clock Modes

Channel Configuration			Clock Source				Control Source					Timer Soure
Clock Mode CCR1 CM2,CM1 CM0	CCR2		BRG	DPLL	REC	TRM	CD	R-Strobe	X-Strobe	F-Sync	Output Via TxCLK	TCP
	TSS	TIO										
0	0	0	-	-	RxCLK	TxCLK	AxCLK	-	-	-	-	TxCLK
1	0	0	-	-	RxCLK	RxCLK	-	AxCLK	TxCLK	-	-	RxCLK
2	0	0	RxCLK	BRG	DPLL	TxCLK	AxCLK	-	-	-	-	TxCLK
2	1	1	RxCLK	BRG	DPLL	BRG/16	AxCLK	-	-	-	BRG/16	BRG/16
3	0	1/0	RxCLK	BRG	DPLL	DPLL	AxCLK	-	-	-	DPLL	DPLL
4	0	0	-	-	OSC	OSC	TxCLK	-	-	-	-	OSC
4	0	1	-	-	OSC	OSC	...	-	-	-	OSC	OSC
5	0	0	-	BRG	RxCLK	RxCLK	TxCLK	(RTSA)	(TTSA)	AxCLK	TS-Control	RxCLK
6	0	0	OSC	BRG	DPLL	TxCLK	-	-	-	-	-	TxCLK
6	1	0	OSC	BRG	DPLL	BRG/16	TxCLK	-	-	-	-	BRG/16
6	1	1	OSC	BRG	DPLL	BRG/16	-	-	-	-	BRG/16	BRG/16
7	0	0	OSC	BRG	DPLL	DPLL	TxCLK	-	-	-	-	DPLL
7	0	1	OSC	BRG	DPLL	DPLL	-	-	-	-	DPLL	DPLL

Note:

1. The maximum permitted serial data rate in an externally clocked operating mode is 8.192 Mb/s. In an internally clocked operating mode with an external reference clock or using internal OSC, the maximum clock rate is 12 MHz (or 19.2 MHz if the scaling factor of the BRG is programmed to 1), and the maximum data rate will be 1200 kbit/s.
2. The ratio between the receive frequency (fr) and the transmit frequency (fx) for a channel must satisfy the condition fr/fx < 3 in Clock Modes 0, 2 and 6; there are no restrictions on phase shift. Slower transmit data rates can be realized with receive and transmit strobes (Clock Mode 1).
3. Clock Modes 4, 6, 7 use the internal OSC and need an external quartz crystal to be connected at the RxCLKA-AxCLKA pins. It is unnecessary to use two separate crystals for two serial channels. Instead it is sufficient to apply a crystal to channel A and provide the reference clock for channel B by externally connecting the AxCLKA and RxCLKB pins. The PT7A6526 also uses the RxCLKA-AxCLKA pins to connect an external quartz crystal.

Figure 13



Normally, 33pF capacitors are used for frequencies below 10MHz and 22pF capacitors for frequencies above 10MHz. Refer to Figure 13.

Bus Configuration

In addition to the point-to-point configuration, the PT7A6526 effectively supports point-to-multipoint (pt-mpt, or bus) configurations by means of Internal Idle and Collision Detection/ Collision Resolution methods.

In a pt-mpt configuration comprising a central station (master) and several peripheral stations (slaves), or in a multimaster configuration, data transmission can be initiated by any station over a common transmission medium (bus). In case multiple stations attempt to transmit data simultaneously (collision), the bus is assigned to one station by a Collision-Resolution procedure implemented by the device. The bus assignment function is based on a priority algorithm having both fixed and rotating priorities that enables each station to access the bus in a time that can be pre-determined. As a result, any number of transmitters can be connected to the serial bus.

Requirements for bus operation are:
- NRZ encoding
- OR connection of data at the bus
- feedback of bus information (CxDA/CxDB input)

The bus configuration is selected via the CCR1 register.

Note: Central clock supply for each station is not necessary if both the receive and transmit clocks are recovered by the DPLL (clock mode 7). In this case, the DPLL also minimizes the phase shift between the transmit clocks of the individual transmitters; so that an opening flag sequence will be sufficient to allow correct collision detection.

The bus mode can be operated independently of the clock mode, e.g., in clock mode 1 (receive and transmission strobe) or clock mode 5 (programmable time-slots).

Bus Access Procedure

The idle state of the bus is identified by eight or more successive 1s. In case of a transmit request in the device, the frame is transmitted, and the bus is identified as busy with the first zero of the opening flag(start flag).

After the frame has been transmitted, the bus becomes available again by transmitting at least eight 1s.

Note: If the bus is occupied by other transmitters and/or there is no transmit request in the device, logic 1 will be continuously transmitted at the TxDA/TxDB output.

Collisions

During the transmission, the data transmitted from the device is compared with the data on the bus. In case that an erroneous bit is detected (log 1 sent and log 0 detected, or vice versa), the frame is immediately aborted, and the idle pattern (logic 1) is transmitted. Transmission will be initiated again by the device as soon as possible.

A transmitted 0 is given priority over a 1 due to the OR connection at the bus, and the individually combined stations in the address field of the transmitted HDLC frame differ from one another. Therefore, the fact that a collision has occurred will be detected during transmission of the address field. The frame of the transmitter with the highest temporary priority (address field number) is not affected and is transmitted without interruptions. All other transmitters terminate operation immediately.

Note: If a wired OR connection has been realized by an external pull-up resistor without decoupling, the data output, (TxDA/ TxDB) can be used as an open drain output and connected directly to the CxDA, CxDB input.

Bus Timing Mode

For bus configuration, the device provides two timing modes, differing only in the period between sending data and evaluation of the transmitted data for collision detection.

- Timing Mode 1 (CCR1: SC1, SC0 = 01)

  At the point on the bus where the transmitter is connected, the beginning of each new bit period is marked by the rising edge of the transmit clock via the TxD pins. The level is evaluated for CD purposes 1/2 clock period later, (half way through the bit period) with the falling clock edge at the CxD pins.

- Timing Mode 2 (CCR1: SC1, SC0 = 11)

  Data is output with the falling clock edge and evaluated with the next falling clock edge. Thus one complete clock period is available during data output and their evaluation.

The following two notes are for Bus Timing Mode 2.

Note 1: In Clock Mode 1 (Strobe), if receiving and transmitting strobes are used on a circuit link, the receiving strobe should be one clock cycle after the transmitting strobe.

Note 2: In Clock Mode 5 (Time-slot), the delay (programmed in RTSA and CCR2) on the receiving end should be one clock later than the delay (programmed in TTSA and CCR2) on the transmitting end.

Data Encoding

In point-to-point configurations, the device supports both NRZ and NRZI data encoding (selectable via CCR1 register).

Accurate recovery of the clock (and consequent identification of the bit boundaries) from received NRZ data is dependent upon an adequate number of transitions per unit time between one bit value to the other. However, the actual *payload* data - which must be arbitrary - can, in general, have any number of log 1s and/or log 0s in a row. In order to prevent confusion between the data being encapsulated and its HEX 7E (01111110) flag, the HDLC system prevents more than five log 1s in a row from being transmitted by inserting extra log 0s into the bit stream as necessary. A useful byproduct of this *bit-stuffing* procedure is the prevention of too many log 1s in a row from being transmitted, but it does nothing to prevent a long string of log 0s from being transmitted. Therefore, prior to feeding data to the HDLC system, specially designed means (such as *whitening, or pseudo-randomizing*) are used to insure that there will not be too many log 0s in a row. At the receive end, the recovered clock allows accurate data recovery. The HDLC system removes the extra log 0s inserted at the transmit end (along with the other HDLC *overhead* information) and sends a bit stream to its host which is identical to what was received from the host at the transmit end. The host then reverses the data *whitening* process.

Unfortunately, none of the above processing prevents six log 1s in a row from being transmitted whenever the HDLC HEX 7E flag is needed. In order to shorten the maximum number of successive same value bits being transmitted from six to five, a further encoding, called *differential* or *NRZI* encoding is performed just prior to transmission. Thus, this type of encoding is especially suitable for Clock Modes 2, 3, 6, and 7, in which the clock is recovered from the received data by means of the DPLL circuits.

Special Functions

Modem Control Functions (RTS/CTS, CD)

The device provides two pins (RTS, CTS) per serial channel supporting the standard of RTS-CTS modem handshaking procedure to control the HDLC transmitters.

Data output is performed with the rising clock edge and data input with the falling edge. A transmit request will be indicated by outputting log 0 at the request-to-send output (RTSA/RTSB). It is also possible to program the RTS outputs by software. After receiving permission to transmit (CTSA/CTSB) the device transmits a frame.

If permission to transmit is withdrawn during the transmission process, the frame is aborted (idle). After new permission to transmit is received and if all of the data are still available in the device, the terminated frame will be re-transmitted (self-recovery) without interrupting the microprocessor. However, if permission to transmit is withdrawn after the 32nd byte in the information field, the transmitter and the XFIFO are reset, the RTS output is deactivated, and an interrupt is generated for the microprocessor.

Carrier Detect (CD) Receiver Control

Similar to the RTS/CTS control for the transmitter, the device supports the carrier detect modem control function for the serial receivers if the Carrier Detect Auto Start (CAS) function is programmed by setting the CAS bit in the XBCH register. CAS function is always available in clock modes 0,2 and 3 via the AxCLK pin, and in clock modes 4,6 and 7 via the TxCLK pin, but only if this pin has been programmed as input by clearing the TIO bit in the CCR2 register. In clock mode 1, the CD function is not supported (see Table 7 for an overview).

If the CAS function is selected, the corresponding HDLC receiver is enabled and data reception is started when a high level is sampled at the CD input.

Receive Length Check Feature

The device offers the possibility to supervise the maximum length of received frames and to terminate data reception in case this length is exceeded.

This feature is controlled via the special Receive Length Check Register (RLCR).

The function is enabled by setting the RC (Receive Check) bit in RLCR and programming the maximum frame length via bits RL6...RL0.

According to the value written to RL6...RL0, the maximum receive length can be adjusted in multiples of 32-byte blocks as follows:

MAX. LENGTH = (RL+1) x 32

All frames exceeding this length are treated as if they have been aborted from the opposite station, i.e., the microprocessor is informed via a
- RME interrupt, and the
- RAB bit in RSTA register is set.

To distinguish the over-length frames from those really aborted from the opposite station, the receive byte count (readable from RBCH, RBCL registers) exceeds the maximum receive length (via RL6...RL0) by one or two bytes in this case.

The check includes all data that are copied into the RFIFO. It does not include the address byte (s) if address recognition is selected. It includes the RSTA value in all operation mode.

One Bit Insertion

Similar to the zero bit insertion (bit-stuffing) as defined by the HDLC protocol, the device offers a completely new feature of inserting/deleting a one after seven consecutive zeros in the transmit/receive data stream if the serial channel is operating in a bus configuration.

This method is profitable if clock recovery should be performed by DPLL.

Since only NRZ data encoding is supported in a bus configuration, there are possibly long sequences without edges in the receive data stream in case of successive “0” s received, and the DPLL may lose synchronization.

Using the one bit insertion feature by setting the OIN bit in the CCR1 register, however, it is guaranteed that at least after
- 5 consecutive “1”-s a “0” will appear (bit-stuffing), and
- 7 consecutive “0”-s a “1” will appear (one insertion),
and thus a correcting function of the DPLL is ensured.

Note: As the bit-stuffing method is fully transparent to the user but not in accordance with the HDLC protocol, it can only be applied in private systems using chip circuits exclusively.

Table 8. RESET Values

Resgister	RESET Value	Description
CCR1	00H	- power down mode serial port configuration; pt-pt, NRZ coding, transmit data pins are open drain outputs - clock mode 0
CCR2	00H	RTS pin normal function - CTS and RFS interrupts disabled, no data inversion
MODE	00H	Auto-mode 1 byte address field external timer mode - receives inactive RTS output controlled by chip, timer resolution: K = 32.768, no test loop
STAR	48H	XFIFO write enable Receive line inactive No commands executing
ISTA EXIR	00H	- No interrupts masked
CMDR	00H	No commands
XBCH RBCH	00H	- interrupt controlled data transfer (DMA disabled) - full-duplex LAPB/LAPD operation of LAP controller - carrier detect auto start of receiver disabled
XCCR RCCR	00H	1-bit time-slot

Operational Description

Reset

The PT7A6526 is forced into the Reset state if HIGH level is input to the RES pin for at least 1.8ms. During RESET, the device is temporarily in the power-up mode, and a subset of the registers is initialized with defined values.

After Reset, the device is in power-down mode. The defined values for the registers are shown in Table 8.

Initialization

After Reset, the microprocessor must write to a minimum set of registers, plus an optional set, depending on the required features and modes of operation.

First, the serial port configuration and the clock mode need to be defined via the CCR1 register. The clock mode must be set before power-up, or simultaneously with power-up.

The microprocessor may switch the device between power-up and power-down modes with no influence upon the contents of the registers; the internal state remains unchanged.

In power-down state, however, all internal clocks and oscillator circuitry are disabled; no interrupts are forwarded to the microprocessor.

This state can be used as standby mode when the device is temporarily not needed, thus greatly reducing the power consumption.

After initialization, the microprocessor switches each individual channel of the PT7A6526 into operational phase by setting the PU bit in the CCR1 register (power-up, if not already done during initialization).

Initially, the microprocessor should bring the transmitter and receiver to a defined state by issuing a XRES (transmitter reset) and RHR (receiver reset) command via the CMDR register. If data reception will be performed, the receiver must be activated by setting the RAC bit in MODE to 1.

If no *Clear to Send* function is provided via a modem, the CTS pin must be connected directly to ground in order to enable data transmission.

Now the device is ready to transmit and receive data. Control of the data transfer phase is performed mainly by commands from microprocessor to device via the CMDR register, and by interrupt indications from device to microprocessor.

Additional status information (which does not trigger interrupts) is available in the STAR register.

Data Transmission

- Interrupt Mode

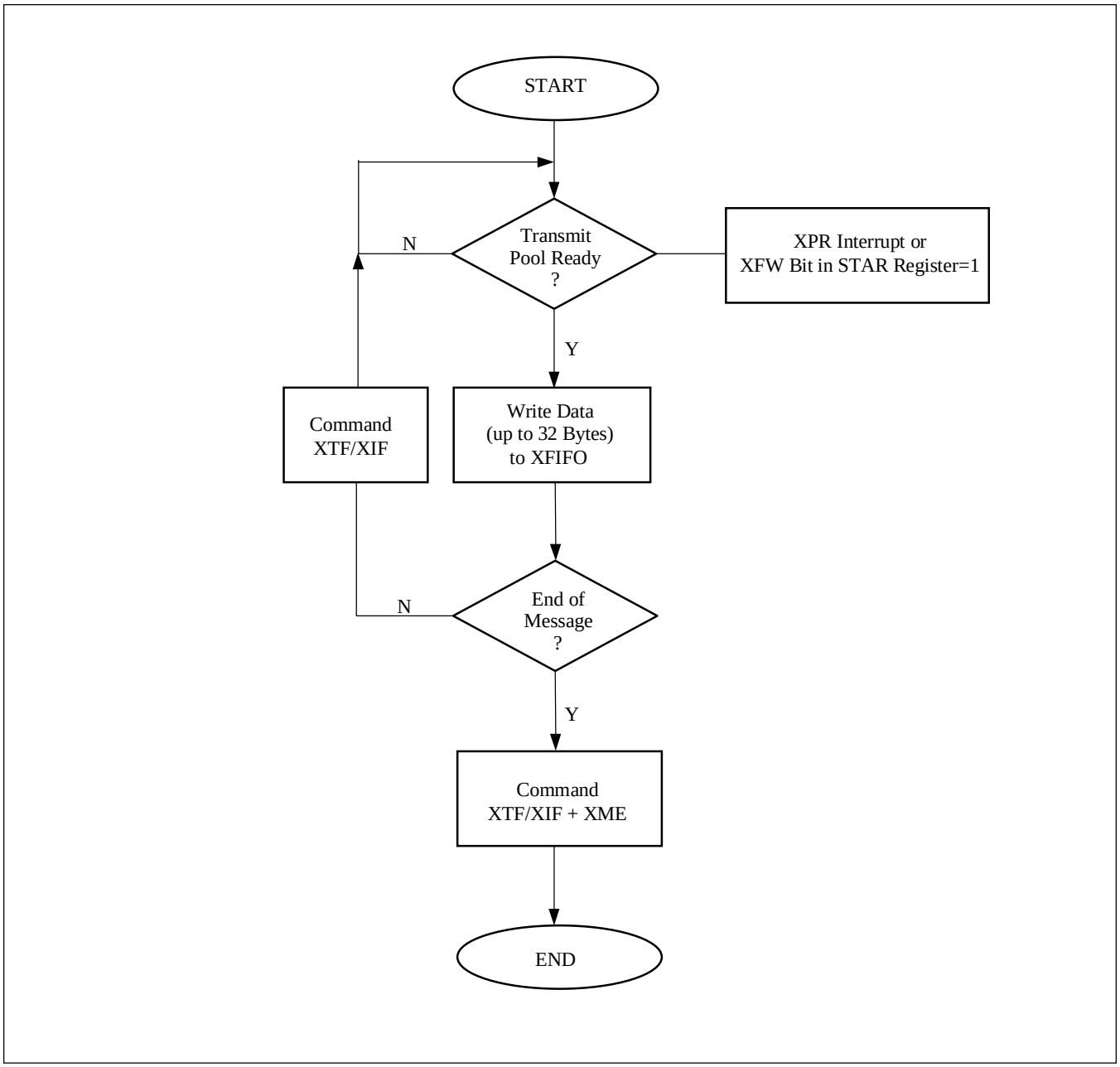
In the transmit direction, 2x32 byte FIFO buffers (transmit pools) are provided for each channel. After checking the XFIFO status by polling the Transmit FIFO Write Enable bit (XFW in STAR register), or after a Transmit Pool Ready (XPR) interrupt, up to 32 bytes may be sent by the microprocessor to the XFIFO.

The transmission of a frame can be started by issuing an XTF or XIF command via the CMDR register. If the transmit command does not include an End of Message indication (CMDR: XME), the device will repeatedly request the next data block using an XPR interrupt, as long as no more than 32 bytes are stored in the XFIFO, i.e., a 32-byte pool is accessible to the microprocessor.

This cycle will be repeated until the microprocessor indicates the end of message command, after which frame transmission is completed appropriately by appending the CRC and closing flag sequence.

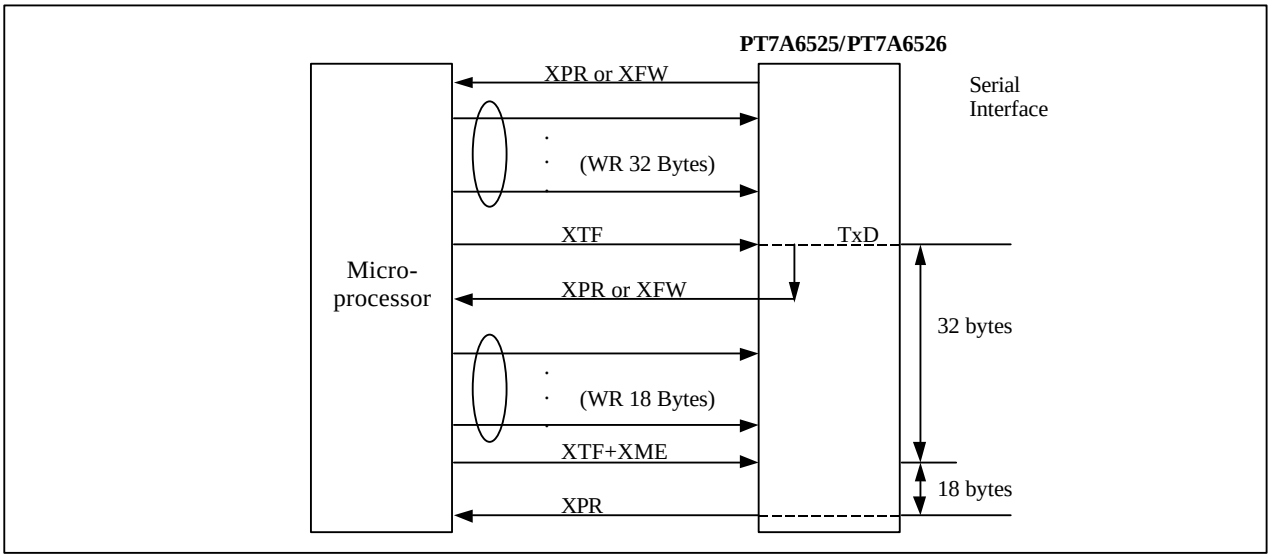
Whenever no more data is available in the XFIFO prior to the arrival of XME, the transmission of the frame is terminated with an abort sequence, and the microprocessor is notified per interrupt (EXIR: XDU). The frame may also be terminated by software (CMDR: XRES).

Figure 14. Flowchart of Frame Transmission in Interrupt Mode



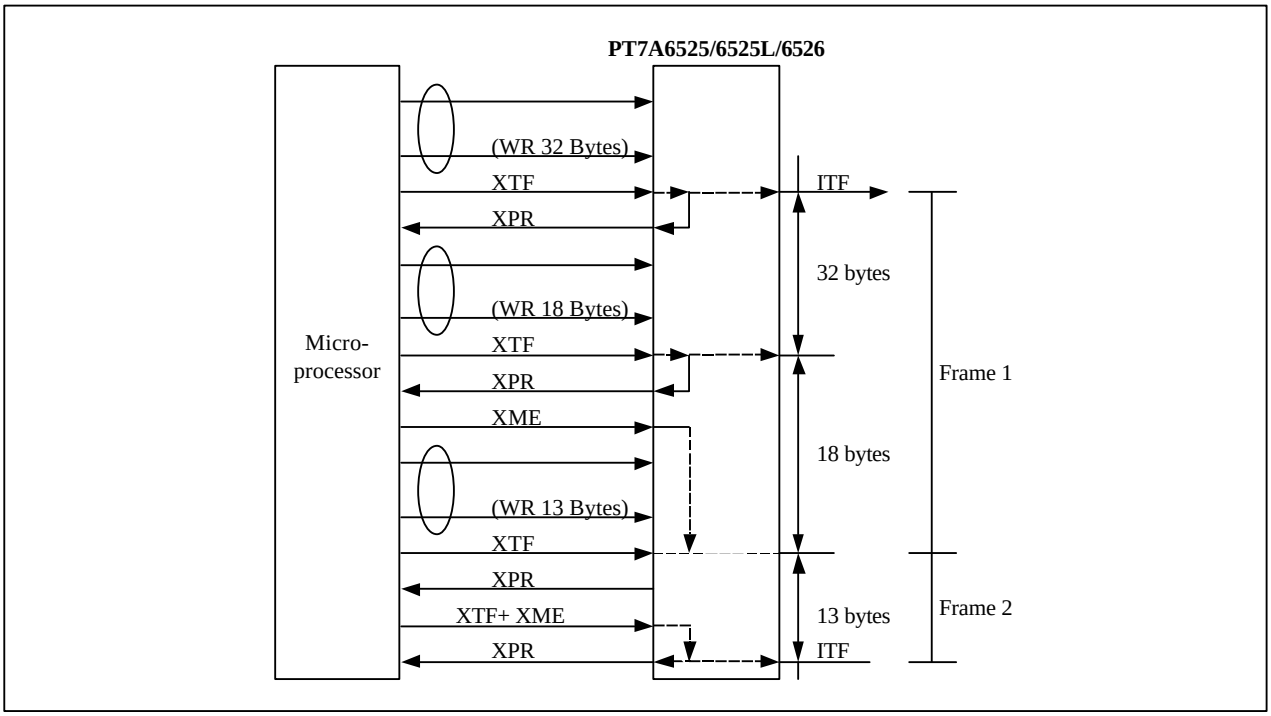
The following figure shows the process of transmitting a 50-byte frame between a microprocessor and a serial interface of a PT7A6525/6525L chip.

Figure 15. Transmission of a 50-byte Frame in Interrupt Mode



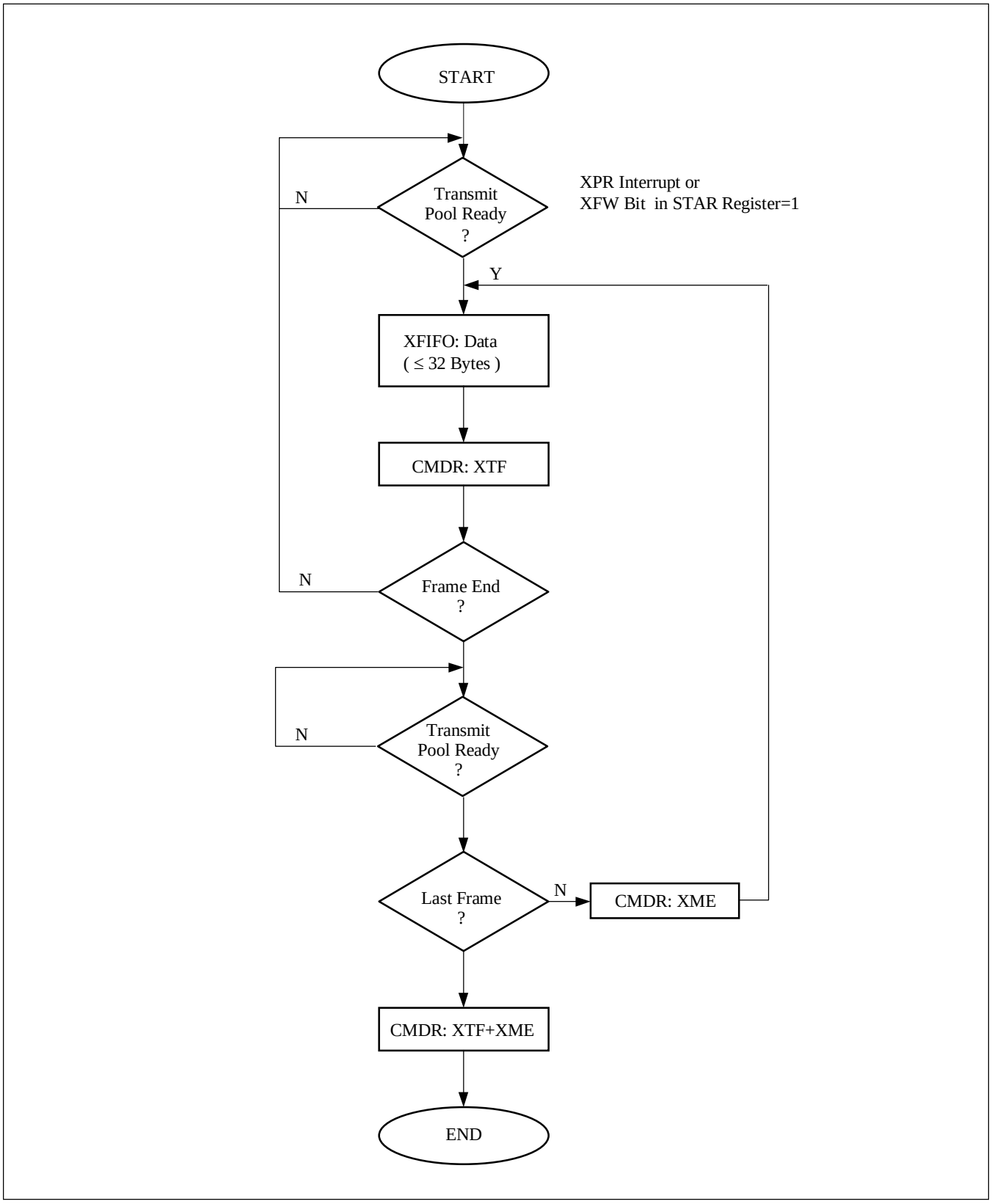
Concatenated frames:
Several frames can be transmitted in a high speed sequence without timefill. The closing flag will be immediately followed by an opening flag. The receiver can even receive frames separated by only one (shared) flag. The following figure shows the process of transmitting two concatenated frames (50 bytes and 13 bytes) to serial interface.

Figure 16. Concatenated Frame Transmission in Interrupt Mode (PT7A6525/6525L/6526)



The following flowchart shows concatenated frame transmission.

Figure 17. Flowchart of Concatenated Frame Transmission in Interrupt Mode



- DMA Mode

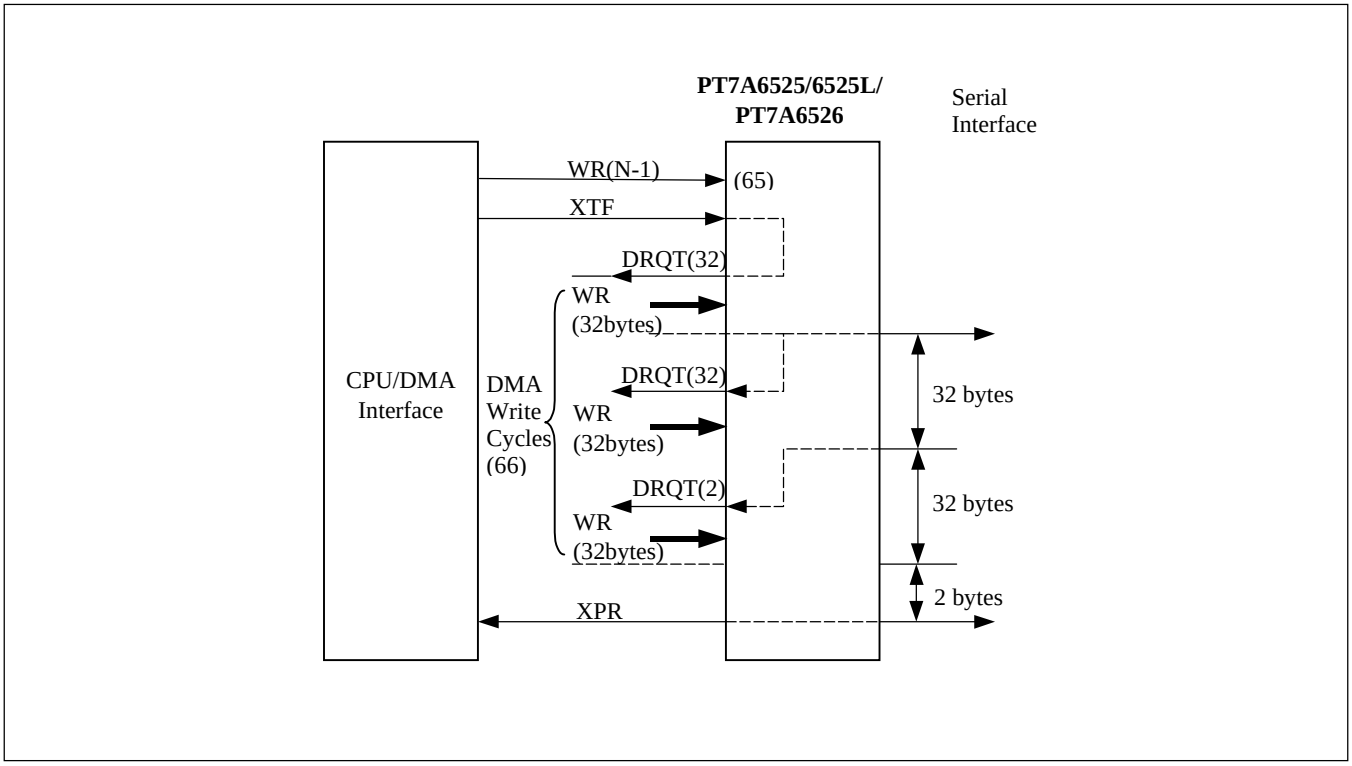
Prior to data transmission, the length of the frame to be transmitted must be programmed via the Transmit Byte Count Registers (XBCH, XBCL). The resulting byte count equals the programmed value plus one byte; as 12 bits are provided via XBCH, XBCL (XBC11...XBC0). Any frame length from 1 to 4096 bytes (4 Kbytes) can be selected.

After this task, data transmission can be initiated by command (XIF or XTF). The device will then autonomously request the correct amount of write bus cycles by activating the DRQT line.

The device will request transmission from the DMA controller for N1+1 times if an N byte frame to be transmitted, thus meeting the N = N1 x 32 + N2 (N1 = 0,1...128, N2 < 32) requirement.

The following figure shows an example of a DMA driven transmission sequence with a supposed frame length of 66 bytes, i.e., programmed transmit byte count (XCNT) equals 65 bytes.

Figure 18. Frame Transmission in DMA Mode



Data Reception

- Interrupt Mode

Also, 2 x 32-byte FIFO buffers (receive pools) are provided for each channel for the receive direction.

There are two different interrupt indications related to the reception of data:

- RPF (Receive Pool Full) interrupt, indicating that a 32-byte block of data can be read from the RFIFO, and the received message is not yet complete.

- RME (Receive Message End) interrupt, indicating that the reception of one message is completed, i.e., either

a. one message of less than 32 bytes, or

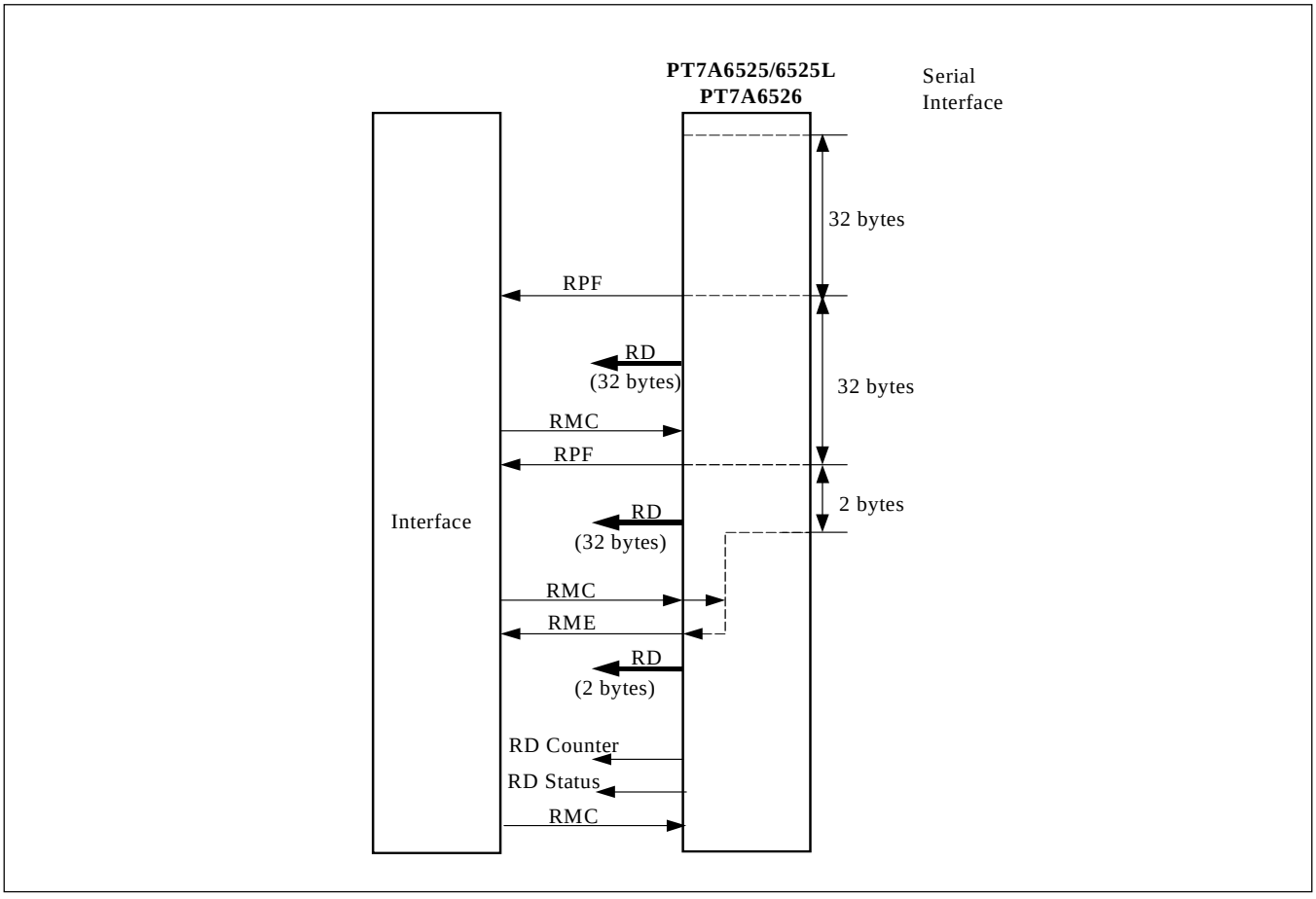
b. the last part of a message having more than 32 bytes is stored in the RFIFO.

After an interrupt has been serviced, or the received data has been read from the RFIFO, the microprocessor must explicitly confirm this fact by issuing an RMC (Receive Message Complete) command.

The microprocessor must service the RPF interrupt before an additional 32 bytes are received via the serial interface, which would cause a *Receive Data Overflow* condition.

The following figure shows the reception process of a 66-byte long frame from the Serial Interface.

Figure 19. Reception of a Long Frame



- DMA Mode

If the RFIFO contains 32 bytes, the device autonomously requests a block data transfer by DMA action of the DRQR line at the start of the 32nd read cycle. This forces the DMA controller to continuously perform bus cycles until 32 bytes are transferred from the device to system memory.

If the RFIFO contains less than 32 bytes (one short frame or the last part of a long frame), the device requests a block data transfer according to the contents of the RFIFO as shown in Table 9.

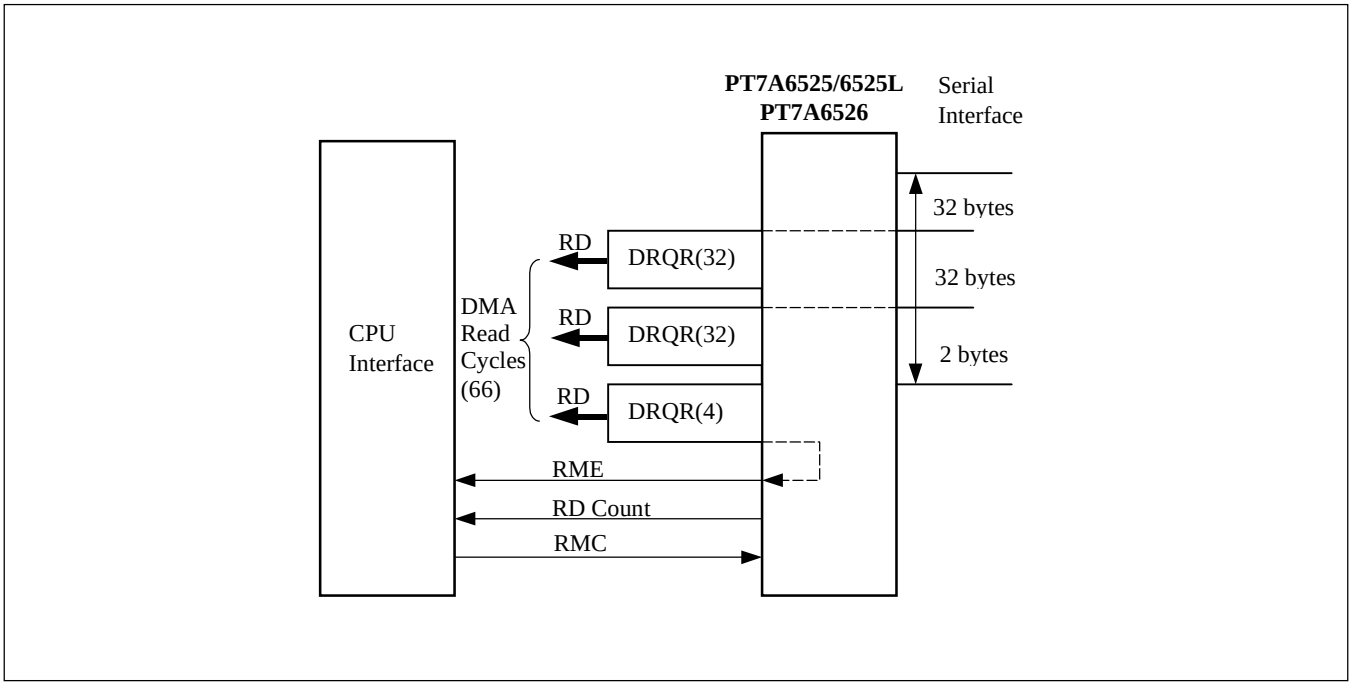
Before starting to receive the next frame, the microprocessor must issue an RMC Command to confirm completion of the present frame`s receive process. Otherwise, the device will not initiate further DMA cycles by activating the DRQR line. It is also possible to set up the DMA controller immediately after the beginning of a frame has been detected by using the RFS Interrupt.

Shown in Figure 20 is an example of an interrupt-controlled reception process, supposing that a long frame (66 bytes) is processed.

Table 9.

	RFIFO Contents (Bytes)	DMA Request (Bytes)
1	1, 2, 3	4
2	4 ~ 7	8
3	8 ~ 15	16
4	16 ~ 32	32

Figure 20. Frame Reception in DMA Mode



Registers

Table 10. Layout of Register Addresses

Address		Register	
A channel	B channel	Read	Write
00 ~ 1F	40 ~ 5F	Receive FIFO Register (RFIFO)	Transmit FIFO Register (XFIFO)
20	60	Interrupt Status Register (ISTA)	Interrupt Mask Register (MASK)
21	61	Status Register (STAR)	Command Register (CMDR)
22	62	Mode (MODE)	
23	63	Timing (TIMR)	
24	64	Extended Interrupt Register (EXIR)	Transmit Address Register 1 (XAD1)
25	65	Receive Byte Count LOW (RBCL)	Transmit Address Register 2 (XAD2)
26	66	-	Receive Address High 1 (RAH1)
27	67	Receive Status Register (RSTA)	Receive Address High 1 (RAH2)
28	68	Receive Address Low 1 (RAL1)	
29	69	Receive HDLC control (RHCR)	Receive Address Low 2 (RALl2)
2A	6A	-	Transmit Byte Count Low (XBCL)
2B	6B	-	Baudrate Generator Register (BRG)
2C	6C	Channel Configuration Register 2 (CCR2)	
2D	6D	Receive Byte Count High (RBCH)	Transmit Byte Count High (XBCH)
2E	6E	Carrier Detect Register(VSTR)	Receive Frame Length Check (RLCR)
2F	6F	Channel Configuration Resgister 1 (CCR1)	
30	70	-	Time-slot Assignment Transmit (TTSA)
31	71	-	Time-slot Assignment Receive (RTSA)
32	72	-	Transmit Channel Capacity (XCCR)
33	73	-	Receive Channel Capacity (RCCR)

Note:
PT7A6526 contains B channel only.

Interrupt Status Register (ISTA)

Table 11. Description of Interrupt Status Register

Bit	Name	Description
D7	Receive Message End (RME)	When it is 1, indicates that one message up to 32 bytes or the last part of a message greater than 32 bytes has been received and is now available in the RFIFO. The message is complete. The actual message length can be determined by reading the RBCH, RBCL registers. Additional information is available in the RSTA register.
D6	Receive Pool Full (RPF)	When it is 1, indicates that a 32-byte block of a message is stored in the RFIFO. The message is not yet completed. Note: This interrupt is generated only in Interrupt Mode.
D5	(Significant in Auto Mode only) (RSC)	When it is 1, indicates that a status change (receive ready/receive not ready) of the opposite station has been detected in auto mode (i.e., the chip has received a RR/RNR supervisory frame in accordance with the HDLC protocol). The current status can be read from the status register (RRNR bit).
D4	Transmit Pool Ready (XPR)	When it is 1, indicates that a data block of up to 32 bytes can be written to the transmit FIFO.
D3	Timer Interrupt (TIN)	When it is 1, indicates that the internal timer and repeat counter are both expired. See description of TIMR register.
D2	Interrupt of Channel A (Channel B only) (ICA)	When it is 1, indicates that an interrupt is caused by channel A, and the interrupt source(s) is (are) indicated in the ISTA register of channel A (i.e., at least one bit of the ISTA register of channel A is set)
D1	Extended Interrupt of Channel A (Channel B only) (EXA)	When it is 1, indicates that an interrupt is caused by channel A, and source(s) is (are) indicated in the EXIR register of channel A.
D0	Extended Interrupt of Channel B (Channel B only) (EXB)	When it is 1, indicates that an interrupt is caused by channel B, and source(s) is (are) indicated in the EXIR register of channel B.

Note:
The ICA, EXA, and EXB bits are present in channel B only and correspond to the ISTA -A, EXIR-A and EXIR -B registers. After the PT7A6526 requests an interrupt by changing its INT pin to logic 0, the microprocessor must first read the ISTA register of channel B and check the state of these bits in order to determine which interrupt source(s) caused the interrupt. Multiple interrupt sources may cause only a single interrupt request.

Mask Register (MASK)

Each interrupt source can be selectively masked by setting the respective bit in MASK (whose bit positions correspond to those in ISTA register). Masked interrupts are not indicated when reading ISTA. Instead, they are internally stored and will be indicated after the corresponding MASK bits are reset.

Note: In the event of an extended interrupt, no interrupt request will be generated with EXA, EXB bits masked, even though this bit is set in ISTA.

Extended Interrupt Register (EXIR)

Table 12. Description of Extended Interrupt Register

Bit	Name	Description
D7	Transmit Message Repeat (XMR)	When 1, indicates that the transmission of the last message has to be repeated because - the chip has received a negative acknowledgement in auto mode, - a collision has occurred after sending the 32nd data byte of a message in a bus configuration, or - CTS (transmission enable) has been withdrawn after sending the 32nd data byte of a message in point-to-point configuration.
D6	Transmit Data Under-run / Extended Transmission End (XDU/EXE)	When 1, indicates that the actual frame has been aborted with IDLE; the XFIFO holds no further data, but the frame is not yet complete. In extended transparent mode, logic 1 of the bit indicates the end of transmission. Note: It is impossible to send transparent, or I frames when a XMR or XDU interrupt is indicated.
D5	Protocol Error (significant in auto-mode only) (PCE)	When 1, indicates that the chip has detected a protocol error, i.e., it has received an - S, or I frame with incorrect N(R), or - S frame containing an I field.
D4	Receive Frame Overflow (RFO)	When 1, indicates that one frame can not be stored due to occupied RFIFO (i.e., the entire frame has been lost). This interrupt can be used for statistical purposes and for indicating that the microprocessor does not respond quickly enough to an incoming RPF or RME interrupt.
D3	Clear to Send Status Change (CSC)	When 1, indicates that a state transition has occurred at the CTS
D2	Receive Frame Start (RFS)	When 1, indicates that the chip has detected the start of a valid frame after a valid address check in the mode of operation providing address recognition, or after the opening flag (transparent mode 0) delayed by two bytes. After RFS interrupt, the contents of - RHCR - RAL1, and - RSTA (D0~D3) are valid and can be read by the microprocessor. This interrupt must be enabled by setting the RIE bit in CCR2.
D1	0	
D0	0	

Status Register (STAR)

Table 13. Description of Status Register

Bit	Name	Description
D7	Transmit Data Overflow (XDOV)	When 1, indicates that more than 32 bytes have been written to the XFIFO
D6	Transmit FIFO Write Enable (XFW)	When 1, indicates that data can be written to the XFIFO. Note: XFW is valid only if CEC = 0.
D5	Transmit RNR (significant in auto mode only) (XRNR)	Indicates the status of the chip. 0 - receiver ready 1 - receiver not ready
D4	Receive RNR (significant in auto mode only) (RRNR)	Indicates the status of the remote station. 0 - receiver ready 1 - receiver not ready
D3	Receive Line Inactive (RLI)	When 1, indicates that neither FLAGs as interframe time fill nor frames are being received via the receive line. Note: Significant in point-to-point configurations.
D2	Command Executing (CEC)	0 - no command is currently being executed, the CMDR register can be written. 1 - a command (written previously to CMDR) is currently being executed; no further commands can be written via CMDR register. Note: CEC will be active at most 2.5 transmit clock periods. If the chip is in power-down state, CEC will stay active.
D1	Clear To Send State CTS	If the CIE bit in CCR2 is set, this bit indicates the state of the CTS pin. 0 - CTS is inactive (high signal at CTS) 1 - CTS is active (low signal at CTS)
D0	Waiting for Acknowledgment (significant in auto mode only) (WFA)	When 1, the chip is in Waiting for Acknowledgement status.

Command Register (CMDR)

Table 14. Description of Command Register

Bit	Name	Description
D7	Receive Message Complete (RMC)	When 1, confirms by microprocessor to chip, that the actual frame or data block has been fetched following an RPF or RME interrupt; thus, the occupied space in the RFIFO can be released. Note: In DMA mode, this command is issued only after an RME interrupt occurs. The chip does not generate further DMA requests prior to the reception of this command.
D6	Reset HDLC Receiver (RHR)	When 1, all data in the RFIFO and the HDLC receiver are deleted. In auto mode, additionally, the transmit and receive sequence number counters are reset.
D5	Receiver Not Ready/ Transmission Repeat (RNR/XREP)	The function of this command depends on the selected modes of operation (MDS1, MDS0, ADM bit in MODE): **Auto mode: RNR** The status of the chip receiver is set. Determines whether a received frame is acknowledged via an RR or RNR supervisory frame in auto mode. 0 - Receiver Ready (RR) 1 - Receiver Not Ready (RNR) **Extended transparent mode 0, 1: XREP** While XTF and XME are set (write 2AH to CMDR), the chip repeatedly transmits the contents of the XFIFO (1~32 bytes) without HDLC framing fully transparent, i.e., without FLAG, CRC insertion and bit stuffing. The cyclic transmission is stopped with an XRES command.
D4	Start Timer (STI)	When it is "1", the internal timer is started. Note: The timer is stopped by rewriting the TIMR register after start.
D3	Transmit Transparent Frame (XTF)	**Interrupt mode** After having written up to 32 bytes to the XFIFO, this command initiates the transmission of a transparent frame. An opening flag sequence is automatically added to the data by the chip. **DMA mode** After having written the length of the frame to be transmitted to the XBCH, XBCL registers, this command (XTF=1) initiates the data transfer from system memory to chip by DMA. Serial data transmission starts as soon as 32 bytes are stored in the XFIFO.
D2	Transmit I Frame (used in auto mode only) (XIF)	When 1, the transmission of an I frame in auto mode will be initiated. In addition to the opening flag sequence, the address and control field of the frame are automatically added by the chip.
D1	Transmit Message End (used in interrupt mode only) (XME)	When 1, indicates that the data block last written to the transmit FIFO completes the actual frame. The chip can terminate the transmission operation properly by appending the CRC and the closing flag sequence to the data. In DMA mode, the end of the frame is determined by the transmit byte count in XBCH, XBCL. This bit must not be set in DMA mode.
D0	Transmit Reset (XRES)	When 1, the contents of the XFIFO are deleted and IDLE is transmitted. This command can be used by the microprocessor to abort a frame currently in transmission. After setting XRES, an XPR interrupt is generated in any case.

Mode Register (MODE)

Table 15. Description of Mode Register

Bit	Name	Description
D7	Mode Select (MSD 1)	To select the HDLC controller mode of operation: - 00 auto mode - 01 non-auto mode - 10 transparent mode - 11 extended transparent mode
D6	Mode Select (MSD 0)	
D5	Address Mode (ADM)	The meaning of this bit varies with the selected mode of operation. **Auto mode, non-auto mode** The length of the HDLC address field is defined. 0 8-bit address field 1 16-bit address field **Transparent mode** 0 Transparent mode 0; no address recognition. 1 Transparent mode 1; high address byte recognition. **Extended transparent mode without HDLC framing** 0 Extended transparent mode 0; received data in RAL1. 1 Extended transparent mode 1; receive data in RFIFO and RAL1. Note: In extended transparent modes, the RAC bit must set to "0" to enable fully transparent reception.
D4	Timer Mode (TMD)	To set the mode of operation of the internal timer: - 0 external mode The timer is controlled by the microprocessor and can be started at any time by setting the STI bit in CMDR. - 1 internal mode The timer is used internally by the chip for time-out and retry conditions in auto mode. Refer to description of TIMR register.
D3	Receive Active (RAC)	- 0 HDLC receiver inactive - 1 HDLC receiver active In extended transparent modes, this bit must be reset to enable fully transparent reception.
D2	Request To Send (RTS)	- 0 The RTS pin is controlled by the chip autonomously. RTS is activated when a frame transmission starts and deactivated after the transmission is completed. - 1 The RTS pin is controlled by the microprocessor. If this bit is set, the RTS pin is activated immediately and remains active until this bit is reset (invalid in bus configuration).
D1	Timer Resolution (TRS)	To select the resolution of the internal timer (factor K, see description of TIMR register): - 0 K = 32768 - 1 K = 512
D0	Test Loop (TLP)	When 1, RxD is disconnected from the mechanical pin and internally connected to TxD of the same channel. TxD pin remains active.

Timer Register (TIMR)

Table 16. Description of Timer Register

Bit	Name	Description
D7 ~ D5	CNT	**Internal timer mode (MODE. TMD = 1)** Retry counter (in HDLC known as N2) CNT indicates the number of S commands (max.6) which are transmitted autonomously by the chip after expiration of period T1 in case an I frame is not acknowledged by the opposite station. If CNT is set to 7, the number of S commands is unlimited. **External timer mode (MODE, TMD = 0)** CNT plus VALUE indicates the time of period T2 after which a timer interrupt will be generated. The period T2 is T2 = 32 x K x CNT x TCP + T1 If CNT is set to 7, a timer interrupt will be periodically generated after the expiration of T1.
D4 ~ D0	VALUE	Sets the time period T1 as follows: T1 = K x (VALUE + 1) x TCP Where - K is the timer resolution factor which is either 32768 or 512-clock cycles depending on the programming of TRS bit in MODE. - TCP is the clock period of transmit data.

Transmit Address Bytes

Whether the address of a frame is one byte or two bytes in length is indicated by the Mode Register ADM bit. When ADM = 0, it is one-byte address. The XAD1 functions as command and XAD2 functions as response in accordance with X.25 LAPB protocol. When ADM = 1, it is a two-byte address. The XAD1 functions as the high byte, and XAD2 functions as low byte.

- Transmit Address 1 (XAD1)

Table 17. Transmit Address 1

Bit	Name	Description
D7 ~ D2	One-byte Address (XAD1)	These bits are part of the one-byte address and function as a command.
	Two-byte Address (XAD1)	These bits are part of the high address byte.
D1	One-byte Address (XAD1)	This bit is part of the one-byte address and functions as a command.
	Two-byte Address Comand/response (XAD1)	This bit, together with the CRI bit in RAH1 register, decides whether the frame to be transmitted functions as a command or response. CRI = 1, C/R = 1: Transmit Command; CRI = 1, C/R = 0: Transmit Response; CRI = 0, C/R = 0: Transmit Command; CRI = 0, C/R = 1: Transmit Response;
D0	One-byte Address (XAD1)	This bit is part of the one-byte address and functions as a command.
	Two-byte Address Expend bit	0 of this bit indicates that there is a low address byte following XAD1.

- Transmit Address 2 (XAD2)

Table 18. Transmit Address 2

Bit	Name	Description
D7 ~ D0	XAD2	For one-byte address, XAD2 functions as the response address. For two-byte address, XAD2 functions as the low address byte.

Receive Address

RAH1, RAH2 Registers are used in Auto Mode, Non-Auto Mode or Transparent Mode 1 when in 2-byte Address Mode. The high-address byte of a received frame is compared with the content of RAH1 or RAH2 register in Auto mode, Non- Auto Mode and Transparent Mode 1.

Note: The content of the RAH1 Register must be 00 when the address is only 1 byte long in Auto Mode.

- Receive Address High 1 (RAH1)

Table 19. Receive Address High 1

Bit	Name	Description
D7 ~ D2	RAH1	These bits are used to compare with the high address byte of a received frame.
D1	CRI	This bit and C/R bit of the RSTA register define whether the received frame is a command or response. CRI = 1, C/R = 0: Received Command CRI = 1, C/R = 1: Received Response CRI = 0, C/R = 1: Received Command CRI = 0, C/R = 0: Received Response
D0	0	

- Receive Address High 2 (RAH2)

Table 20. Receive Address High 2

Bit	Name	Description
D7 ~ D2	RAH2	These bits are used to compare with the high address byte of a received frame.
D1	Modulo select bit (MCS)	This bit adjusts the control field formats according to the HDLC protocol. - 0 Basic operation (modulo 8) - 1 Extended operation (modulo 128) Note: When modulo 128 is selected in auto mode, the RHCR Register contains compressed extended control field information.
D0	0	

- Receive Address Low 1 (RAL1)

Table 21. Receive Address Low 1

Bit	Name	Description
D7 ~ D0	RAL1	- Auto/non-auto mode (16-bit address) - WRITE only: RAL1 can be programmed with value of the first individual low address byte.
		- Auto/non-auto mode (8-bit address) - WRITE only: According to X.25 LAPB protocol, the address in RAL1 is recognized as the COMMAND address.
		- Transparent mode 1 (high address byte recognition) - READ only: RAL1 contains the byte following the high byte of the address in the receive frame(i.e., the second byte after the opening flag).
		- Transparent mode 0 (no address recognition) - READ only: RAL1 contains the first byte after the opening flag (first byte of receive frame).
		- Extended transparent modes 0, 1 - READ only: RAL1 contains the actual data byte currently assembled at the RxD pin, by passing the HDLC receiver (fully transparent reception without HDLC framing).

- Receive Address Low 2 (RAL2)

Table 22. Receive Address Low 2

Bit	Name	Description
D7 ~ D0	RAL2	For two-byte address, RAL2 functions as low address byte.
		For one-byte address, RAL2 functions as response address in accordance with X.25 protocol.

Receive Status Register (RSTA)

Table 23. Description of Receive Status Register

Bit	Name	Description
D7	Valid Frame (VFR)	1-Valid, 0-Invalid. An invalid frame is either - a frame which is not an integer multiple of 8 bits (n 8 bits) in length (eg. 25 bit) or - a frame which is too short for the mode of operation selected via MODE (MDS1, MDS0, ADM) as follows: · Auto/non-auto mode (16-bit address): 4 bytes · Auto/non-auto mode (8-bit address): 3 bytes · Transparent mode 1:3 bytes. · Transparent mode 0:2 bytes. Note: Shorter frames are not reported.
D6	Receive Data Overflow (RDO)	A data overflow has occurred within the actual frame. Caution: Data is lost, because the microprocessor did not service the RME or RPF interrupt in time.
D5	RC compare/check (CRC)	- 0 CRC check failed; received frame contains errors. - 1 CRC check OK; received frame is error-free.
D4	Receive Message Aborted (RAB)	The received frame was aborted by the transmitting station. In accordance with the HDLC protocol, this frame must be discarded by the microprocessor.
D3 ~ D2	High Byte Adress compare (HA1, HA0)	Significant only if 2-byte address mode is selected. In operating modes with high address byte recognition, the chip compares the high byte of a 2-bytes address with the contents of two individual programmable registers (RAH1, RAH2) and the fixed values FEH and FCH (group address). According to the result of this comparison, the following bit combinations are possible: - 10 RAH1 has been recognized - 00 RAH2 has been recognized - 01 group address has been recognized Note: If RAH1, RAH2 contain the identical values, the combination 00 will be omitted.
D1	Command/Response (C/R)	Significant only if 2-byte address mode is selected. Interpretation of the C/R bit values (bit D1 of high address byte) in the received frame depends on the setting of the CRI bit in the RAH1 register. Refer to the description of RAH1 register.
D0	Low Byte Adress Compare (LA)	Not significant in transparent and extended transparent modes. The low address byte of a 2-byte address field, or the single address byte of a 1-byte address field is compared with two programmable registers (RAL1, RAL2): - 0 RAL2 has been recognized. - 1 RAL1 has been recognized. In accordance with the X.25 LAPB protocol, RAL1 is interpreted as a COMMAND and RAL2 is interpreted as a RESPONSE.

Note:
RSTA corresponds to the last received HDLC frame; it is duplicated in the RFIFO for every frame (last byte of frame).

Receive HDLC Control Register (Read) (RHCR)

The value of the HDLC control field corresponds to the last received frame.
Note: RHCR is duplicated in the RFIFO for every frame.

Table 24. Description of Receive HDLC Control Register

Mode	Contents of RHCR	
	Modulo 8 (MCS = 0)	Modulo 128 (MCS = 1)
Auto mode, one-byte address (U frames) (Note 1)	Control field	Control field (Note 2)
Auto mode, one-byte address (U frames) (Note 1)	Control field	Control field (Note 2)
Auto mode, one-byte address (U frames) (Note 1)	Control field	Control field in compressed form (Note 3)
Auto mode, one-byte address (U frames) (Note 1)	Control field	Control field in compressed form (Note 3)
Non-auto mode, one-byte address	The second byte after flag	
Non-auto mode, two-byte address	The third byte after flag	
Transparent mode 1	The third byte after flag	
Transparent mode 0	The second byte after flag	

Note:
1. S frames are handled automatically and are not transferred to the microprocessor.
2. For U frames (bit 0 of RHCR = 1), the control field is as in the modulo 8 case.
3. For I frames (bit 0 of RHCR = 0), the compressed control field has the same format as in the modulo 8 case, but only the three LSBs of the receive and transmit counters are visible.

Table 25. Content of I frame in RHCR Register

Bit	Name	Description
D7 ~ D5	N(R)	The number of a transmitted frame by Remote Station.
D4	P	- 0 The received I frame needs no response. - 1 The received I frame needs a response.
D3 ~ D1	N(S)	The number of a received frame by Remote Station.
D0	0	-

Tramsmit Byte Count Low (XBCL)

Table 26. Tramsmit Byte Count Low

Bit	Name	Descriptin
D7 ~ D0	XBC7 ~ XBC0	This register is used only in DMA mode. These bits, together with XBC8 ~ XBC11 in XBCH Register, determine the length(1...4095 bytes) of the next frame to be transmitted. The actual length of a frame to be transmitted is XBC+1. If XBC = 0, exactly one byte will be transmitted. The value of XBC allows the chip to request the correct amount of DMA cycles after a XIF or XTF command from CMDR.

Transmit Byte Count High (XBCH)

Table 27. Transmit Byte Count High

Bit	Name	Description
D7	DMA Mode (DMA)	To select the device's mode of data transfer to system memory. - 0 Interrupt controlled data transfer (interrupt mode) - 1 DMA controlled data transfer (DMA mode)
D6	Normal Response Mode (NRM)	Valid and used in auto mode only. It is reset in non-auto mode, transparent mode, and extended transparent mode. - 0 full-duplex LAPB/LAPD operation - 1 half-duplex NRM operation
D5	Carrier Detect Auto Start (CAS)	When set, a high at the CD(AxCLK) pin enables the respective receiver, and data reception is started. Note: CAS has to be "0" for clock modes 1 and 5. In Externed Transparent Mode, this bit is disable.
	Transmit Continuously (XC)	Valid only when DMA mode is selected. If the XC bit is set, the chip continuously requests transmit data, ignoring the transmit byte count programmed via XBCH, XBCL.
D3 ~ D0	Transmit Byte Count (most significant bits) (XBC11 ~ XBC8)	Valid only if DMA mode is selected. Together with XBC7...XBC0, programs the frame length.

BR Generator Register (BGR)

Table 28. Description of BR Generator Register

Bit	Name	Description
D7 ~ D0	BR7 ~ BR0	The value N(0 ~ 1023) - determined by this byte and BR8, BR9 bits in CCR2 - is used to adjust the division factor K: K = (N+1) x 2

Receive Byte Count Low (RBCL)

Table 29. Receive Byte Count Low

Bit	Name	Description
D7 ~ D0	RBC7 ~ RBC0	These bits together with RBC8-RBC11 in RBCH Register determine the length(1...4095 bytes) of the actual received frame. The microprocessor must read this register after each RME Interrupt.

Receive Byte Count High (RBCH)

Table 30. Receive Byte Count High

Bit	Name	Description
D7	DMA Mode (DMA)	The meaning of these bits is the same as that of respective bits in XBCH except that these bits can be read in this register (see XBCH).
D6	XBCH D6 (NRM)	
D5	XBCH D5 (CAS)	
D4	Counter Overfolw (OV)	More than 4095 bytes received. The received frames exceeded the byte count in RBC11,...,RBC0.
D3 ~ D0	Byte Count (most significant bits) (RBC11 ~ RBC8)	Together with RBCL (bits RBC7...RBC0), the received frame can be determined.

Receive Length Check Register (RLCR)

Table 31. Description of Receive Length Check Register

Bit	Name	Description
D7	Receive Check (on/off) (RC)	- 0 receive length check feature disabled - 1 receive length check feature enabled Note: All bytes stored in the RFIFO are relevant for the receive length check feature, including the receiver status byte.
D6 ~D0	Receive Length (RL6 ~ RL0)	The maximum receive length after which data reception is suspended can be programed here. Depending on the value RL programmed via RL6...RL0, the receive length is (RL+1) x 32 bytes. A frame exceeding this length is treated as if it were aborted by the opposite station (RME Interrupt, RAB bit set). In this case, the Receive Byte Count (RBCH, RBCL) is greater than the programmed receive length.

Channel Configuration Register 1 (CCR1)

Table 32. Description of Channel Configuration Register 1

Bit	Name	Description
D7	Switching between Power-Up and Power-Down modes (PU)	- 0 power down (standby) - 1 power up (active)
D6 ~D5	Serial Port Configuration (SC1 SC0)	- 00 NRZ data encoding - 10 NRZI data encoding - 01 bus configuration, timing mode 1 - 11 bus configuration, timing mode 2 Note: If bus configuration is selected, only NRZ coding is supported.
D4	Output Driver Select (ODS)	To define the function of the transmit data pins (TxDA, TxDB) - 0, TxD pins are open drain outputs. - 1, TxD pins are push-pull outputs. Note: Since in time-slot oriented systems the TxD pins are not tristated automatically out of the programmed time-slot, they should be configured as open drain in such systems.
D3	Interframe Time Fill/One Insertion (ITF/OIN)	The function of this bit varies with the selected serial port configuration (bit SC0) . **ITF in point-to-point configuration** To determine the idle (no data to send) state of the transmit data pins (TxDA, TxDB): - 0, Continuous IDLE sequences are sent (TxD pin remains in the "1" state). - 1, Continuous FLAG sequences are sent ("01111110" bit patterns). **OIN in bus configuration** In bus configuration, the ITF is explicitly set to 0, i.e., continuous "1"s are transmitted, and data encoding is NRZ. When this bit is set, a "ONE" insertion (deletion) mechanism is activated, inserting a "1" after seven consecutive "0"s in the transmit data stream and deleting a "1" in the receive data stream. Similar to the HDLC's bit-stuffing mechanism (inserting a "0" after five consecutive "1"s), this method proves to be advantageous when the receive clock is recovered from the receive data stream by means of DPLL, because, whenever a long "0" sequence occurs, it is guaranteed that at least after seven bits a transition occurs in the receive data.
D2 ~ D0	Clock Mode (CM2, CM1, CM0)	To select one of the 8 different clock modes: - 000 clock mode 0 . . . . . . - 111 clock mode 7

Transmit Time-slot Assignment register (Write) (TTSA)

Table 33. Description of Transmit channel assignmant register

Bit	Name	Description
D7 ~ D2	Time-slot Number Transmit (TSNX)	Selects one of up to 64 possible time-slots (00H ~3FH) in which data is transmitted. The number of bits per time-slot can be programmed via XCCR.
D1 ~D0	Transmit Clock Shift, Bit 2-1 (XCS2, XCS1)	Together with the XCS0 in CCR2, the transmit clock shift can be adjusted.

Note: This register is used in clock mode 5 only.

Receive Time-slot Assignment Register (Write) (RTSA)

Table 34. Description of Receive Channel Assignment Register

Bit	Name	Description
D7 ~ D2	Time-slot Number Receive (RSNX)	Defines one of up to 64 possible time-slots (00H -3FH) in which data is received. The number of bits per time-slot can be progrmmed via RCCR.
D1 ~D0	Receive Clock Shift, Bit2-1 (RCS2 , RCS1)	Together with bit RCS0 in CCR2, the receive clock shift can be adjusted.

Note: This register is used in clock mode 5 only.

Transmit Channel Capacity Register (Write) (XCCR)

Table 35. Description of Transmit Channel Capacity Register

Bit	Name	Description
D7 ~ D0	Transmit Bit Count, Bit7- 0 (XBC7 ~ XBC0)	Defines the number of bits to transmitted within a time-slot: Number of bits = XBC + 1. (1... 256 bits/time-slot)

Note: This register is used in clock mode 5 only.

Receive Channel Capacity Register (Write) (RCCR)

Table 36. Description of Receive Channel Capacity Register

Bit	Name	Description
D7 ~ D0	Receive Bit Count, Bit7- 0 (RBC7 ~ RBC0)	Defines the number of bits to be received within a time-slot: Number of bits = RBC + 1. (1... 256 bits/time-slot)

Note: This register is used in clock mode 5 only.

Channel Configuration Register 2 (CCR2)

The meaning of the individual bits in CCR2 depends on the selected clock mode via CCR1 as follows:

Table 37. Description of Channel Configuration Register 2

Bit	Name	Description
D7 ~ D6	Special Output Control (SOC1, SOC0) / Baudrate (BR9, BR8)	**SOC1 SOC0 in clock mode 0,1,4,5** · In bus configuration, the function of pin RTS can be defined by these two bits: - 00 RTS output is activated during transmission of a frame . - 10 RTS output is always high (RTS disabled). - 11 RTS indicates the reception of a data frame (active low). · In point-to-point configuration (selected via CCR1) the 2 bits define data transmission direction among RxDA, RxDB, TxDA and TxDB pins. - 0X, data is transmitted on TxD, received on RxD pin (normal case). - 1X, data is transmitted on RxD, received on TxD pin. **BR9, BR8 in clock mode 2,3,6,7.** Together with BGR register, they define Baudrate Division Factor.
D5	Transmit Clock Shift (XCS0) / Baudrate Division Factor (BDF)	**The bit is set to 0 when in clock mode 0,1,4.** **BDF in clock mode 2,3,6,7** - 0, The division factor of the baudrate generator is set to one (constant). - 1, The division factor is adjusted with BR9 and BR0 bits in CCR2 and BRG register. **XCS0 in clock mode 5.** Together with XCS2 and XCS1 in TTSA register, the bit can adjust transmit clock shift.
D4	Receive Clock Shift (RCS0) / Transmit Clock Source Select (TSS)	**The bit is set to 0 when in clock mode 0,1,3,4,7.** **TSS when in clock mode 2,6.** - 0, The transmit clock is delivered to TCLKA/TCLKB pins. - 1, The transmit clock is derived from the baudrate generator after being divided by 16. **RCS0 in clock mode 5**. Together with RCS2 and RCS1 in RTSA register, the bit adjusts receive clock shift.
D3	Transmit Clock Input /Output switch (TIO)	**The bit is set to 0 when in clock mode 0 and 1.** **Named as TIO when in clock mode 2 through 7.** - 0, TCLKA, TCLKB pins are inputs - 1, TCLKA, TCLKB pins are outputs
D2	Clear To Send Interrupt Enable (CIE)	Any state transition at the CTS input pin may cause an interrupt which is indicated in the EXIR register (CSC bit). The actual state at the CTS pin can be determined by reading the CTS bit of the STAR register. - 0, disable - 1, enable
D1	Receive Frame Start Interrupt Enable (RIE)	When 1, the RFS interrupt (via EXIR) is enabled.
D0	Data Inversion	Valid only when NRZ data encoding is selected. Inverted data is transmitted and received.

Carrier Detect Register (VSTR)

Table 38. Description of Carrier Detect Register

Bit	Name	Description
D7	Carrier detect(CD)	The bit shows the inverted data at the CD (AxCLK or TxCLK) pin even when CAS in Transmit Byte Count High Register (XBCH) is not enabled. Refer to 'Clock Modes' Section of this datasheet.
D4 ~ 60	0	-
D0 ~ D3	version	101

Detailed Specifications

Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc)	-0.3V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.3V to +7.0V
DC Input Voltage	-0.3V to +7.0V
DC Output Current	60mA
Power Dissipation	2W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Sym	Description		Min	Typ	Max	Units
V_{CC}	Supply Voltage	PT7A6525/PT7A6526	4.5	5.0	5.5	V
		PT7A6525L	3.0	3.3	3.6	
T_A	Operating Temperature		-40	25	85	°C

DC Electrical Chacarteristics

Table 39. DC Electrical Chacarteristics

Sym	Description	Test Conditions	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage		2.4	2.0		V
V_{IL}	Input LOW Voltage			1.1	0.8	V
V_{OH}	Output HIGH Voltage - All Pins Except TxD, RxD, INT	PT7A6525/6526, I_{OH}= -12mA	2.5	3.7		V
		PT7A6525L, I_{OH}= -4mA	2.5	3.0		V
V_{OH}	Output HIGH Voltage - Pins RxD, TxD	PT7A6525/6526, I_{OH}= -18 mA	2.5	3.5		V
		PT7A6525L, I_{OH}= -8mA	2.5	3.0		V
V_{OL}	Output LOW Voltage - All Pins Except TxD, RxD, INT	I_{OL}= 3 mA		0.3	0.5	V
V_{OL}	Output LOW Voltage - Pins TxD, RxD, INT	I_{OL}= 5 mA		0.3	0.5	V
I_L	Input Leakage Current	V_I = 0 ~5.5V except AxCLK, RxCLK of PT7A6525L, V_I = 0 ~3.6V for AxCLK, RxCLK of PT7A6525L			±10	µA
I_{OH}	Output HIGH Current - All Pins Except TxD, RxD, INT	PT7A6525/6526, V_{OH}= 4.0V	-6	-10		mA
		PT7A6525L, V_{OH}= 3.0V	-2	-4		mA
I_{OL}	Output LOW Current - Except Pins TxD, RxD, INT	PT7A6525/6526, V_{OL}= 1.0V	6	10		mA
		PT7A6525L, V_{OL}= 0.3V	3	4		mA
I_{OH}	Output HIGH Current - Pins RxD, TxD	PT7A6525/6526, V_{OH}= 4.0V	-10	-15		mA
		PT7A6525L, V_{OH}= 3.0V	-3	-5		mA
I_{OL}	Output LOW Current - Pins TxD, RxD, INT	PT7A6525/6526, V_{OL}= 1.0V	10	15		mA
		PT7A6525L, V_{OL}= 0.3V	6	8		mA
V_{IKH}	Input Clamp Diode Voltage	I_{IN}= 18mA	V_{CC} +0.5		V_{CC} +1.0	V
V_{IKL}	Input Clamp Diode Voltage	I_{IN}= -18mA	GND -0.5		GND -1.0	V
I_{OZH}	Output HIGH Impedence Leakage- Pins TxD, RxD, and INT	V_{OUT}= 0 ~V_{CC}			±10	µA
V_{IKDPH}	Clamp Diode Voltage of Power off	V_{CC}= GND I_{IN}= 18mA	0.5		1	V
V_{IKDPL}	Clamp Diode Voltage of Power off	V_{CC}= GND I_{IN}= -18mA	-0.5		-1	V
V_H	Input Hysteresis Voltage			0.7		V

Note:
Typical figures are at 25 ^{O}C and are for design aid only; not production tested.

Power Supply and Capacitance Characteristics

Table 40. Power Supply and Capacitance Characteristics

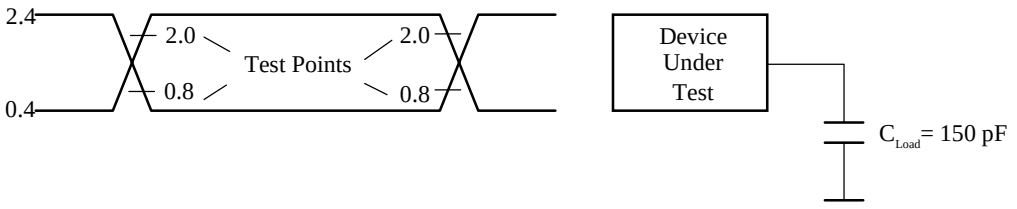
Sym	Description	Test Condition		Min	Typ	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	$\overline{CS}$ = $V_{CC,}$ other input pin = GND, output open, power down (set D7 of CCR1 = 0)				200	μA
I_{CCD}	Power Supply Current when Power Down	RxCLK = 4.096MHz, AxCLK = 8KHz, $\overline{CS}$ = $V_{CC,}$ other input pin = GND, output open, power down (set D7 of CCR1 = 0)	6525/6526			1.5	mA
			6525L			1.0	
I_{CC}	Power Supply Current	RxCLK = 4.096MHz, AxCLK = 8KHz, $\overline{CS}$ = $V_{CC,}$ Other Input Pin = GND, Output Open, Power Up	6525/6526			8	mA
			6525L			4	
C_{IN} *	Input Capacitance	V_{IN} = 0V			8		pF
C_{OUT} *	Output Capacitance	V_{OUT} = 0V			10		pF

Note:

1. V_{CC} = 5V ± 5% for PT7A6525/6526, V_{CC} = 3.3V ± 5% for PT7A6525L.
2. Typical figures are at 25 °C and are for design aid only; not production tested.

AC Electrical Characteristics

Figure 21. Input/Output Waveform for AC Tests



Note :

T_A = -40 to 85 °C; V_{CC} = 5 V ±5%

Inputs are driven to 2.4V for a logical “1” and to 0.4 V for a logical “0”. Timing measurements are made at 2.0V for a logical ‘1” and at 0.8 V for a logical ‘0”.

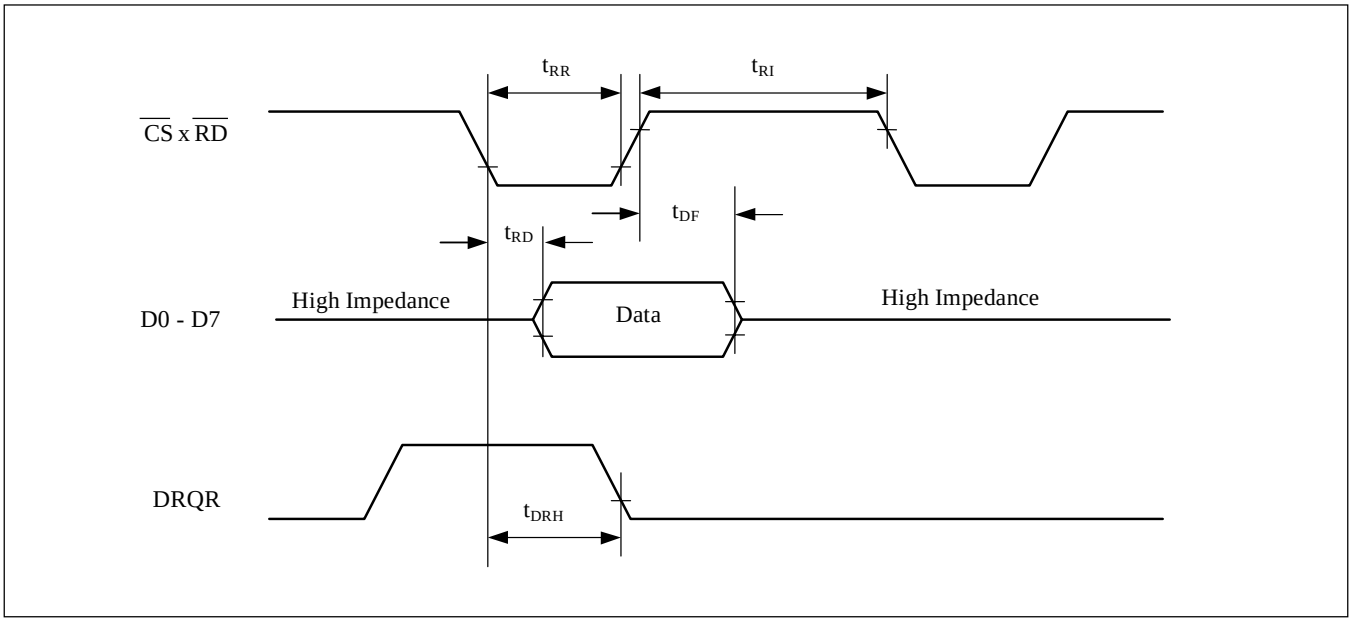
Microprocessor Interface Timing

Table 41. Characteristics of Interface Timing

Sym	Description	Test Conditions	Min	Typ	Max	Units
t_{AA}	ALE pulse width		25			ns
t_{AL}	Address setup time to ALE		10			ns
t_{LA}	Address hold time from ALE		10			ns
t_{ALS}	Address latch setup time to $\overline{WR}$, $\overline{RD}$		0			ns
t_{AS}	Address setup time to $\overline{WR}$, $\overline{RD}$		10			ns
t_{AH}	Address hold time from $\overline{WR}$, $\overline{RD}$		10			ns
t_{DRH}	DMA request delay				90	ns
t_{RR}	$\overline{RD}$ pulse width		70			ns
t_{RD}	Data output delay from $\overline{RD}$				70	ns
t_{DF}	Data float delay from $\overline{RD}$				25	ns
t_{RI}	$\overline{RD}$ control interval		35			ns
t_{WW}	$\overline{WR}$ pulse width		60			ns
t_{DW}	Data setup time to $\overline{WR}$ x $\overline{CS}$/$\overline{DS}$ x $\overline{CS}$		10			ns
t_{WD}	Data hold time from $\overline{WR}$ x $\overline{CS}$/$\overline{DS}$ x $\overline{CS}$		10			ns
t_{WI}	$\overline{WR}$ control interval		60			ns
t_{DSD}	$\overline{CS}$*$\overline{DS}$ delay after R/$\overline{W}$ set up		0			ns

- Microprocessor Interface Timing in Bus Mode

Figure 22. Diagram of Microprocessor Interface Timing in Intel Bus Mode (in Read Cycle)



Note: If DACKA/B is provide by the DMA controller, the CS and DS is not needed to cause the falling of the DRQR signal. Refer to Page 7, Table 2, the description of DACKA and DACKB.

Figure 23. Diagram of Microprocessor Interface Timing in Intel Bus Mode (in Write Cycle)

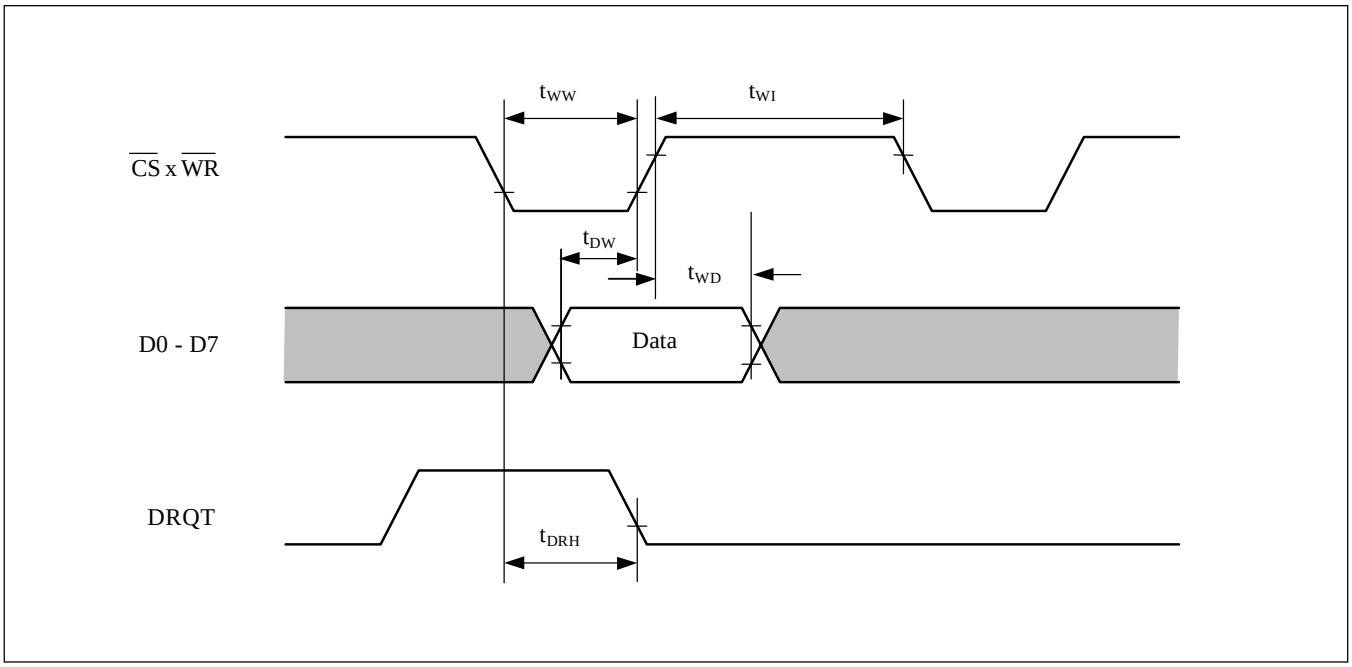


Figure 24. Multiplexed Address Timing

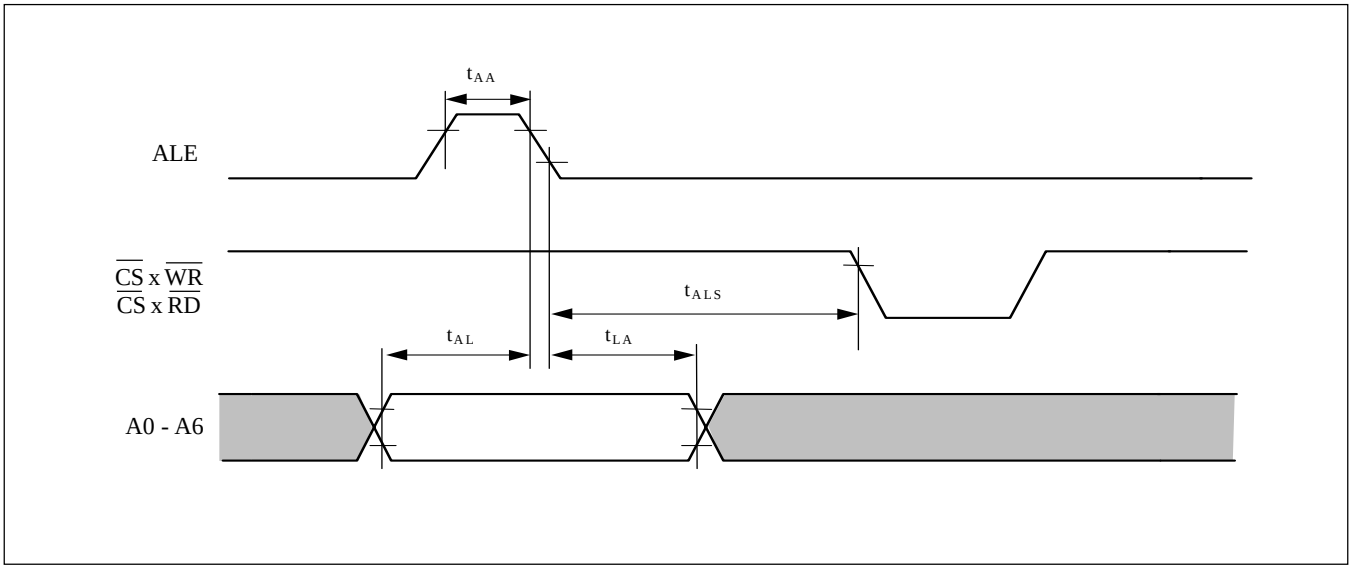
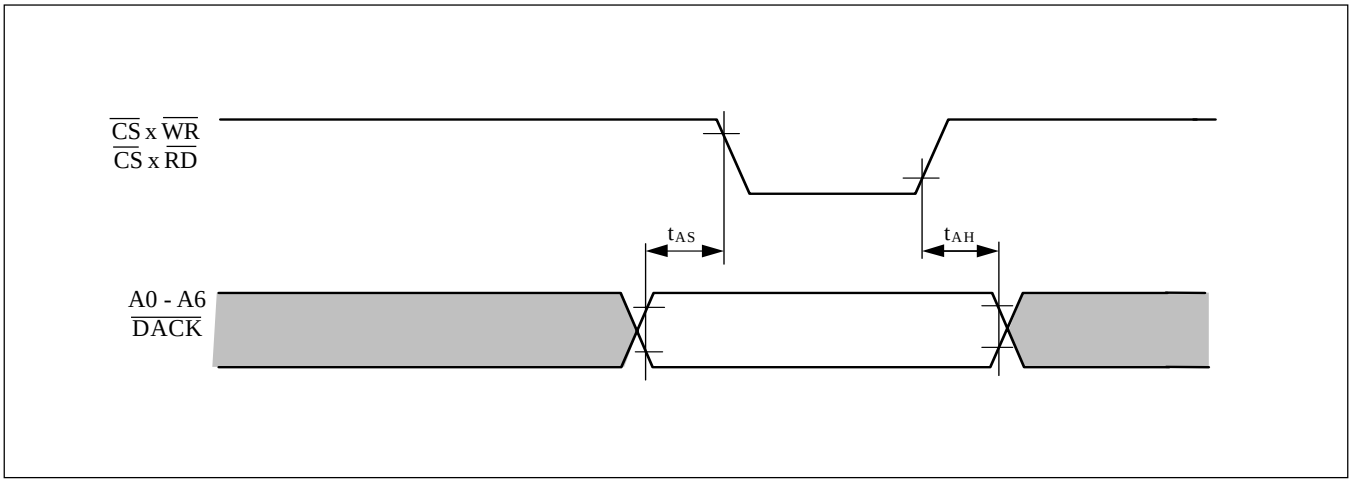


Figure 25. Address Timing



- Microprocessor Interface Timing in Motorola Bus Mode

Figure 26. Diagram of Microprocessor Interface Timing in Motorola Bus Mode (in Read Cycle)

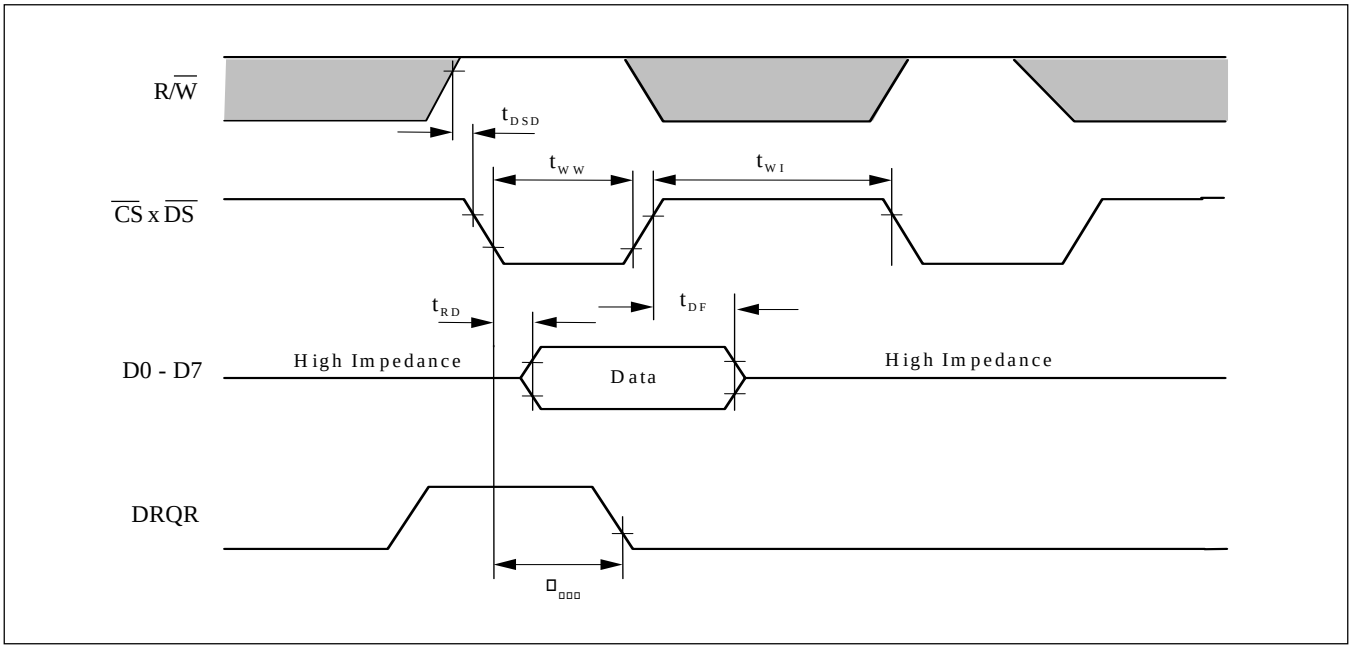


Figure 27. Diagram of Microprocessor Interface Timing in Motorola Bus Mode (in Write Cycle)

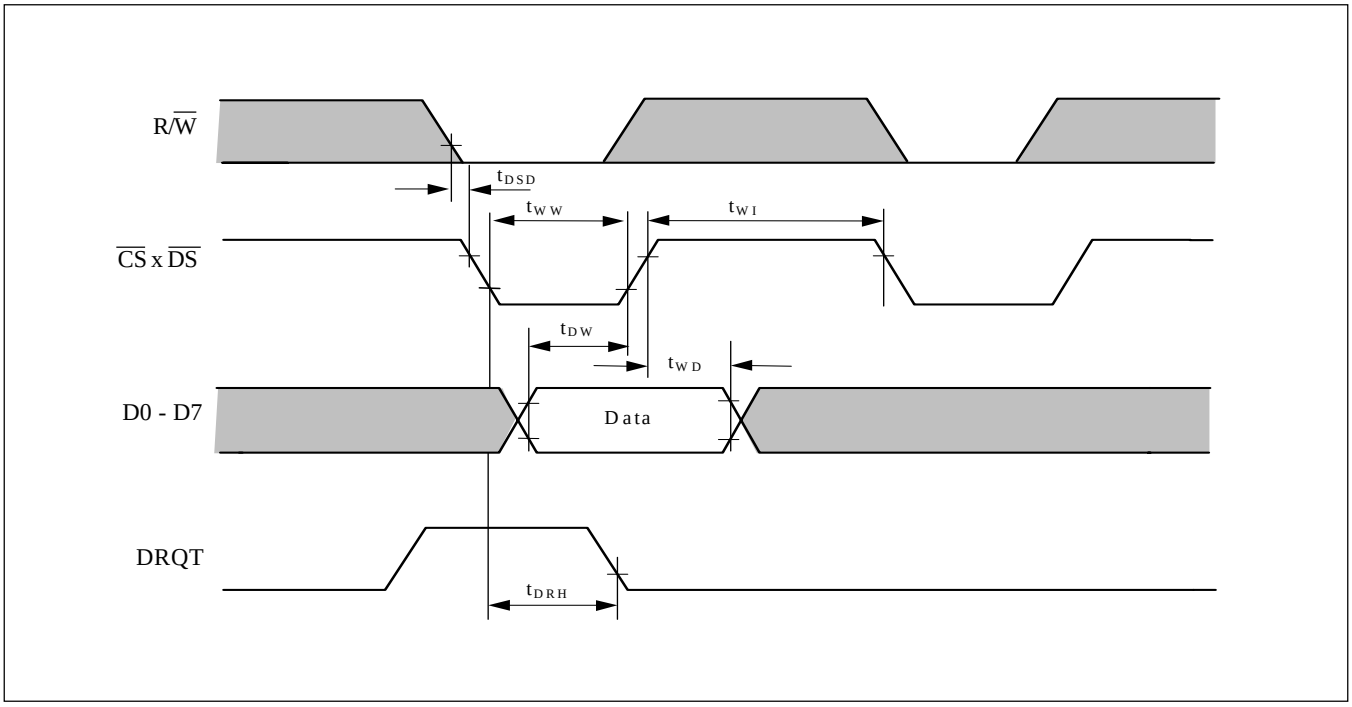
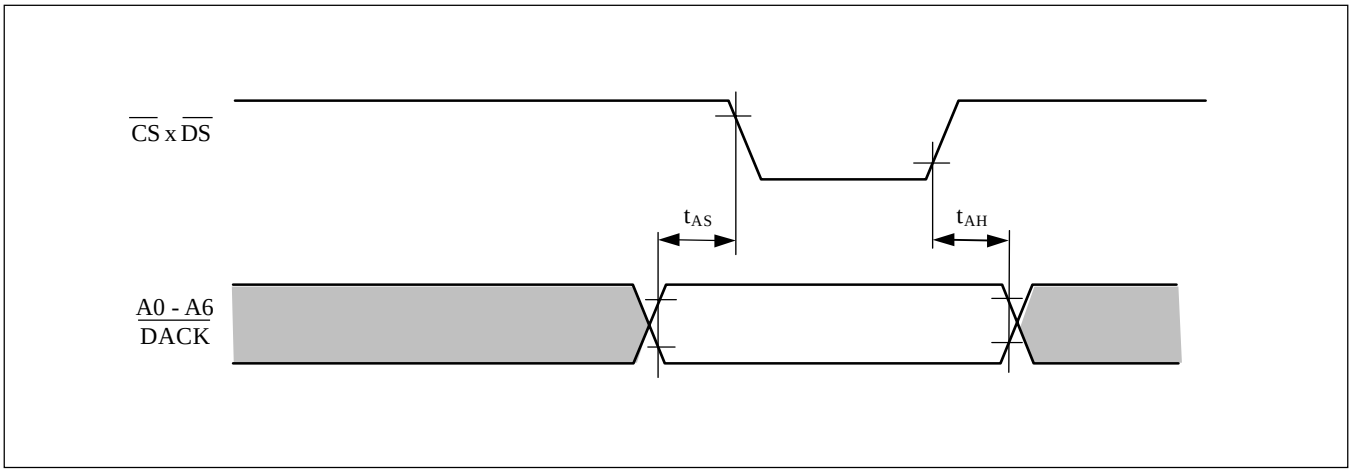


Figure 28. Address Timing

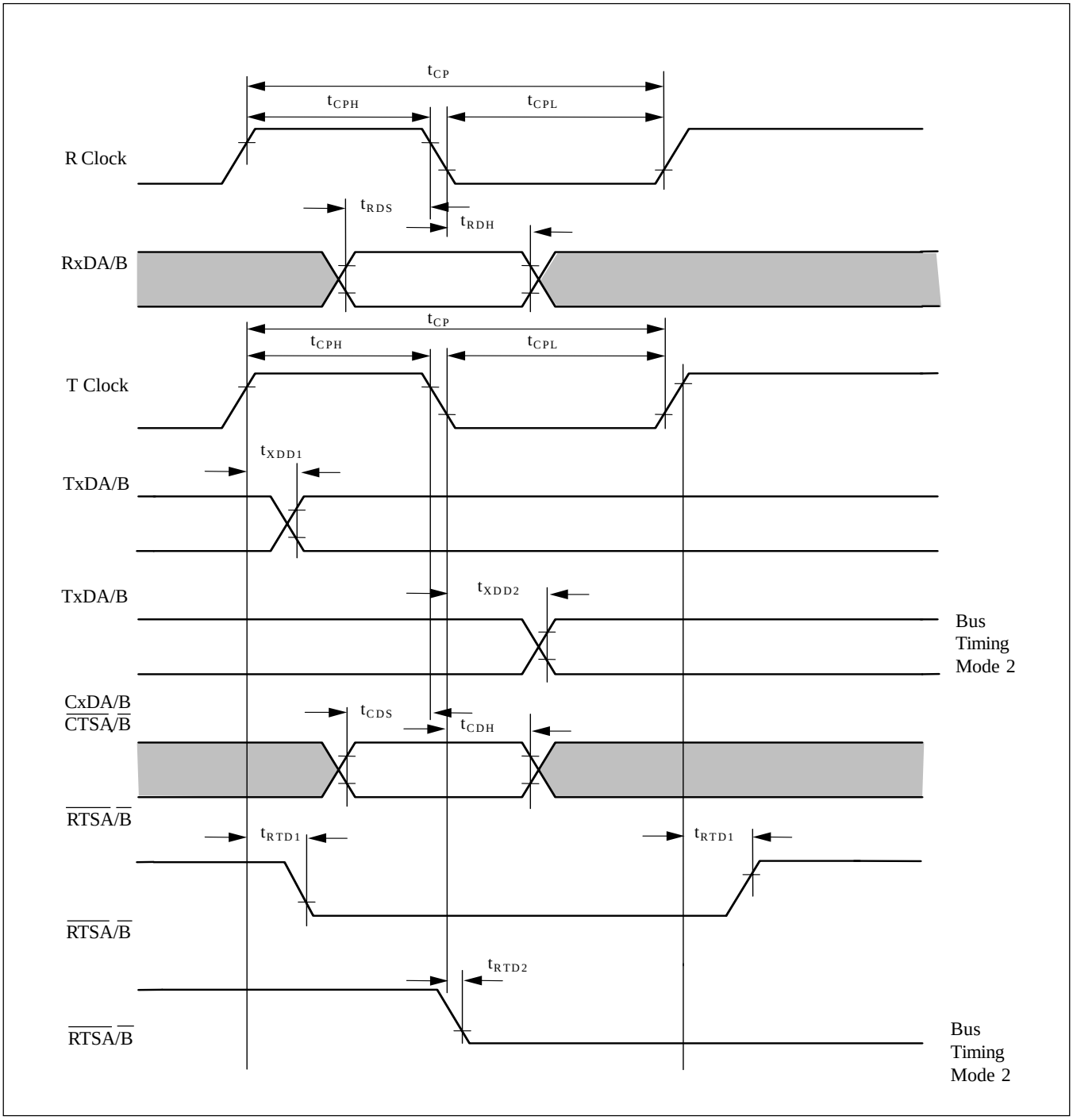


Serial Interface Timing

Table 42. Characteristics of Serial Interface Timing

Sym	Description	Test Condition	Min	Typ	Max	Units
t_{RDS}	Receive data setup		20			ns
t_{RDH}	Receive data hold		5			ns
t_{CDS}	Collision data setup		5			ns
t_{CDH}	Collision data hold		30			ns
t_{XDD2}	Transmit data delay, falling clock edge		20		75	ns
t_{XDD1}	Transmit data delay, rising clock edge		10		75	ns
t_{RTD1}	Request to send delay 1		10		120	ns
t_{RTD2}	Request to send delay 2		10		85	ns
t_{CP}	Clock period		120			ns
t_{CPL}	Clock period LOW		50			ns
t_{CPH}	Clock period HIGH		50			ns

Figure 29. Serial Interface Timing

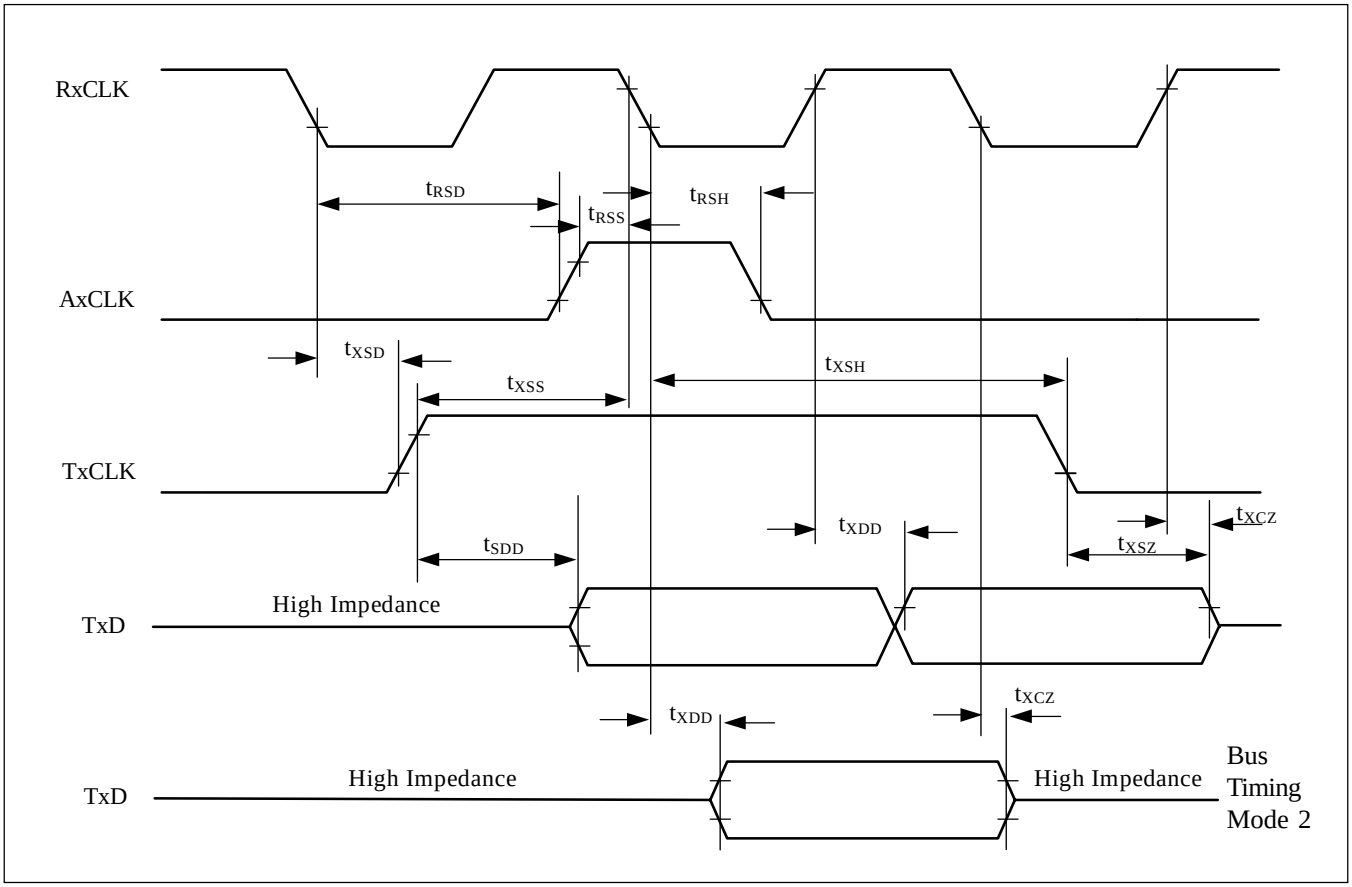


Strobe Timing

Table 43. Characteristics of Strobe Timing(Clock Mode 1)

Sym	Description	Test Conditions	Min	Typ	Max	Unit
t_{RSD}	Receive strobe delay		30			ns
t_{RSS}	Receive strobe setup		60			ns
t_{RSH}	Receive strobe hold		30			ns
t_{XSD}	Transmit strobe delay		30			ns
t_{XSS}	Transmit strobe setup		60			ns
t_{XSH}	Transmit strobe hold		30			ns
t_{XDD}	Transmit data delay				68	ns
t_{SDD}	Strobe data delay				90	ns
t_{XCZ}	High impedance from clock				50	ns
t_{XSZ}	High impedance from strobe				50	ns

Figure 30. Diagram of Strobe Timing (Clock Mode 1)

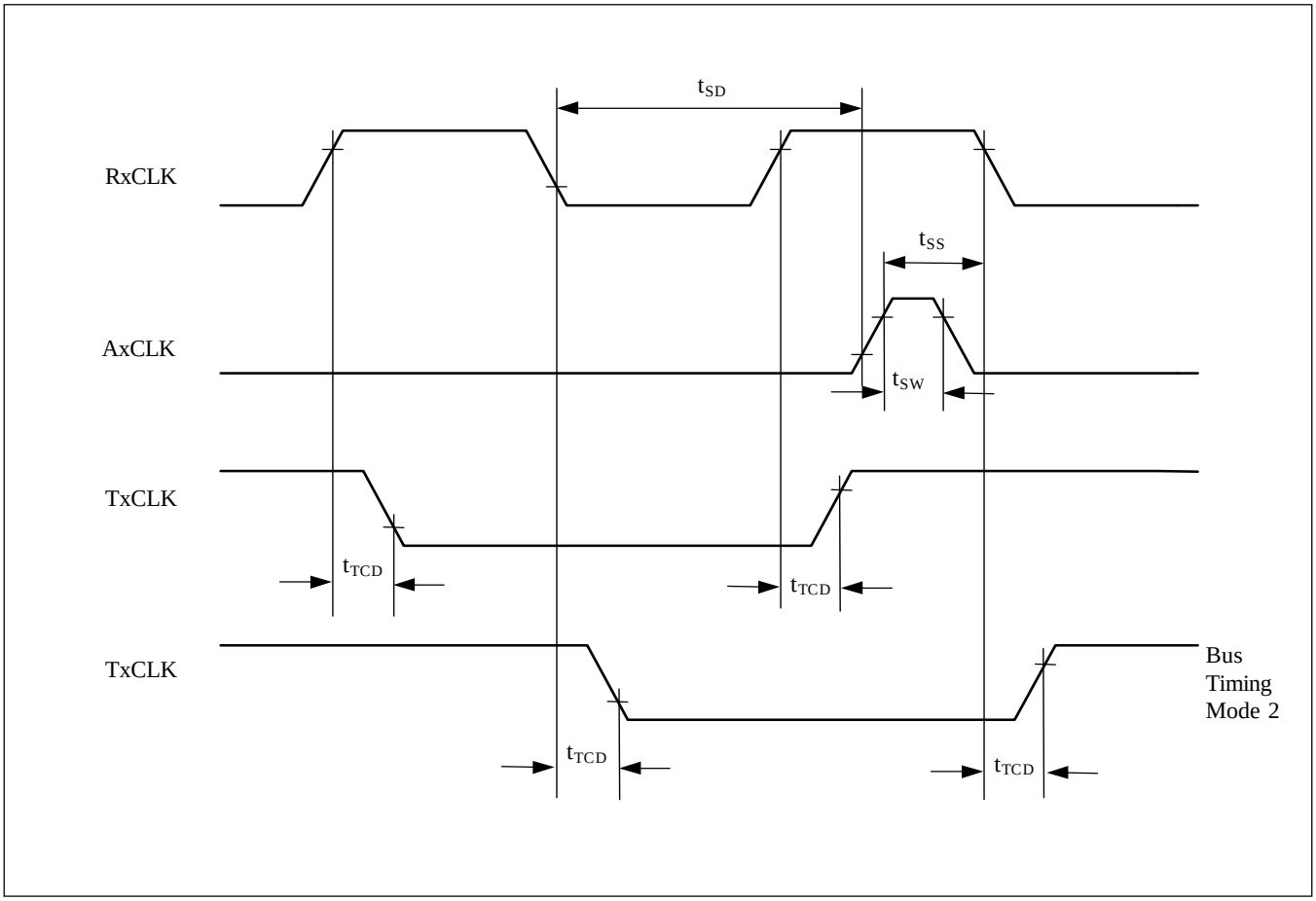


Synchronization Timing

Table 44. Characteristics of Synchronization Timing (Clock Mode 5)

Sym	Description	Test Conditions	Min	Typ	Max	Units
t_{SD}	Sync pulse delay		30			ns
t_{SS}	Sync pulse setup		30			ns
t_{SW}	Sync pulse width		40			ns
t_{TCD}	Time-slot control delay		10		75	ns

Figure 31. Diagram of Synchronization Timing (Clock Mode 5)



Internal Clocking(Clock Mode 2, 3, 6, 7)

Table 45. Table . Internal Clocking (Clock Mode 2, 3, 6, 7)

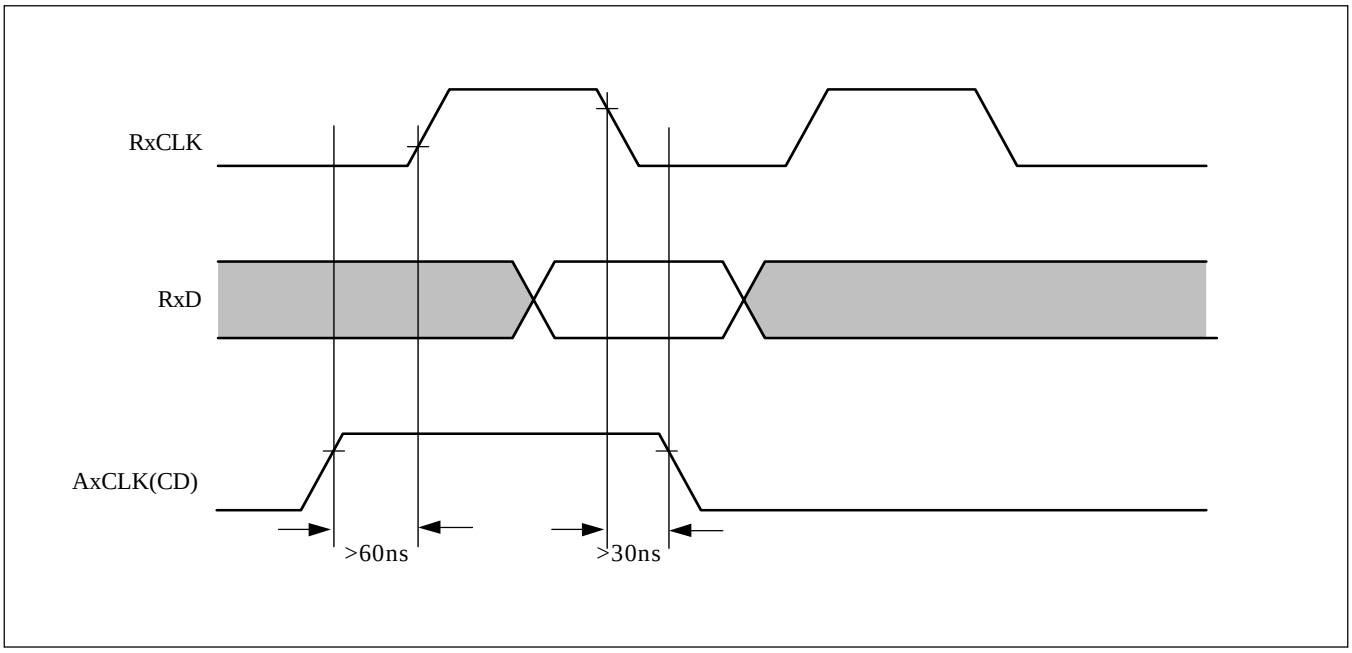
Sym	Description	Test Conditions	Min	Typ	Max	Unit
f_{CLK}	Clock frequency Baudrate generator used				19.3	MHZ
f_{CLK}	Clock frequency Baudrate generator not used				12.3	MHZ

RESET Timing

Table 46. reset Characteristics

Sym	Description	Test Conditions	Min	Typ	Max	Unit
t_{RWH}	RESET HIGH		1800			ns

Figure 32. Diagram of CD Timing



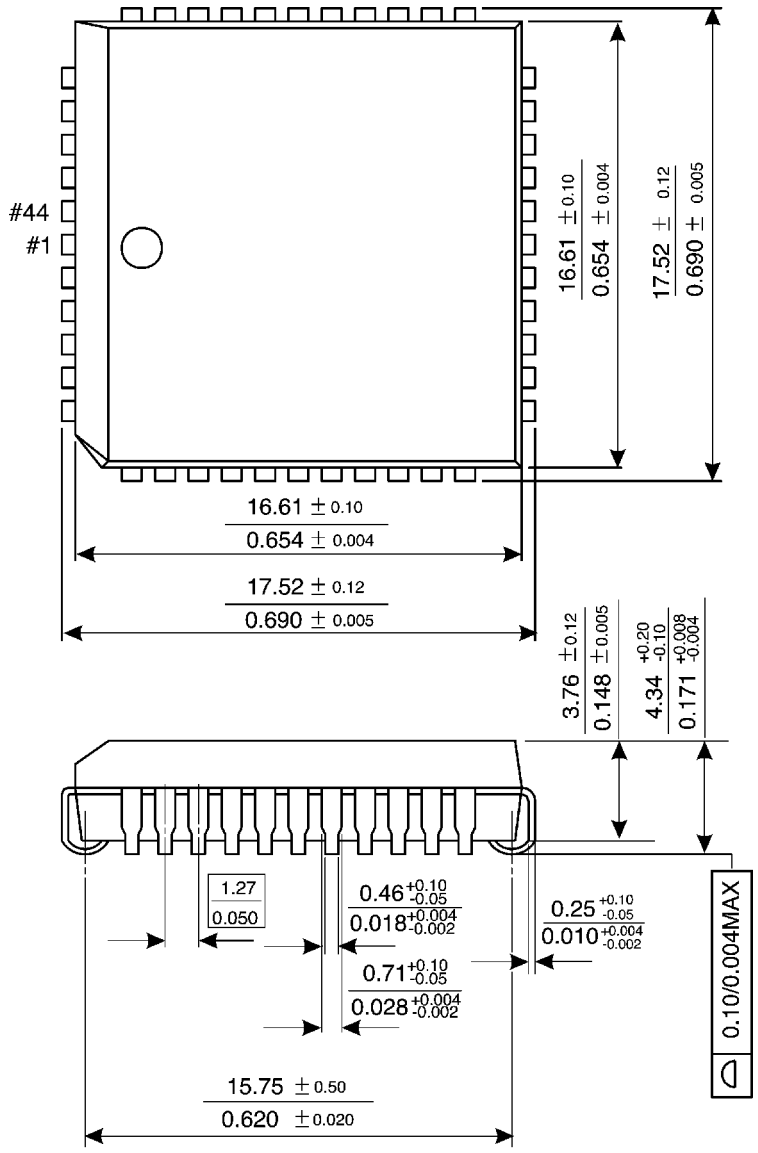
Quartz Crystal Specifications

Characteristics of Quartz Crystals for the PT7A6525/6525L/6526

• Mode of oscillation	parallel resonant
• Frequency calibration tolerance	50 ppm
• Frequency shift during lifetime	10 ppm
• Temperature coefficient/frequency drift	50 ppm within the temperature range
• Motional capacitance	15 pF ± 20%
• Effective serial resistance	≤ 50 Ω for 19.2 MHz
• Shunt capacitance	≤ 7 pF
• Drive level	1 mW
• Recommended case type	HC - 49/U (ANSI - standard)

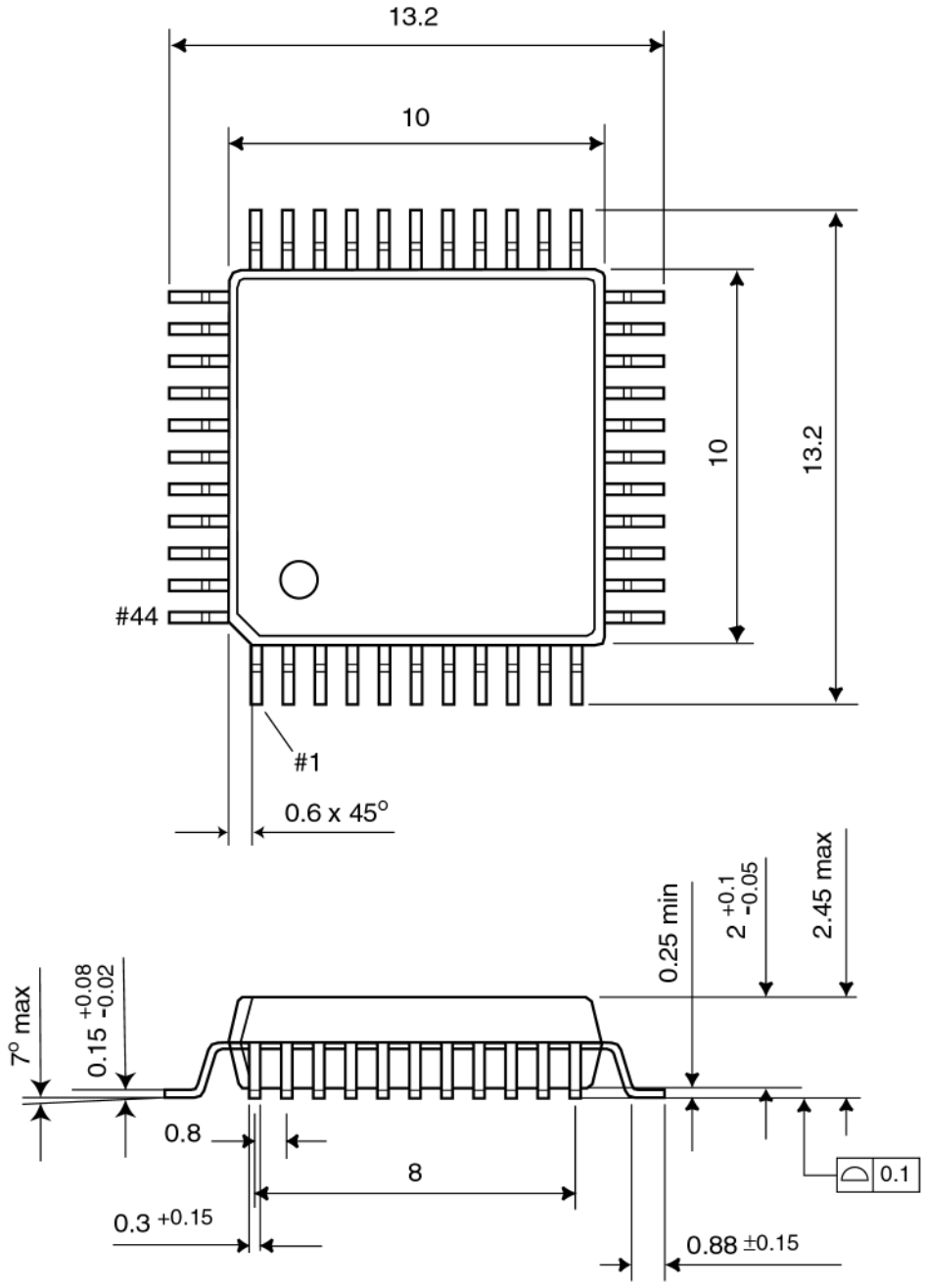
Mechanical Information

Figure 33. 44-Pin PLCC



Dimensions in Millimeters/Inches

Figure 34. 44-Pin MQFP



Dimension in Millimeters

Appendix: Index of Registers

Table 48. Index of Registers of PT7A6525/6525L/6526

Notes

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